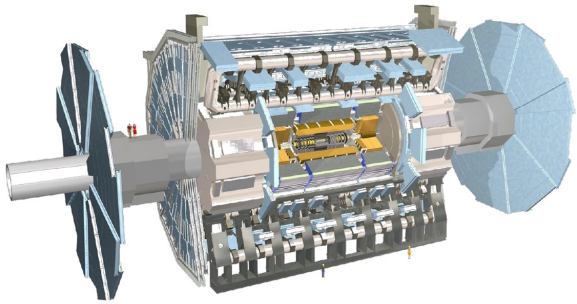


The ATLAS Phase-II Upgrade Program

Martin Kocian *for the ATLAS Collaboration*

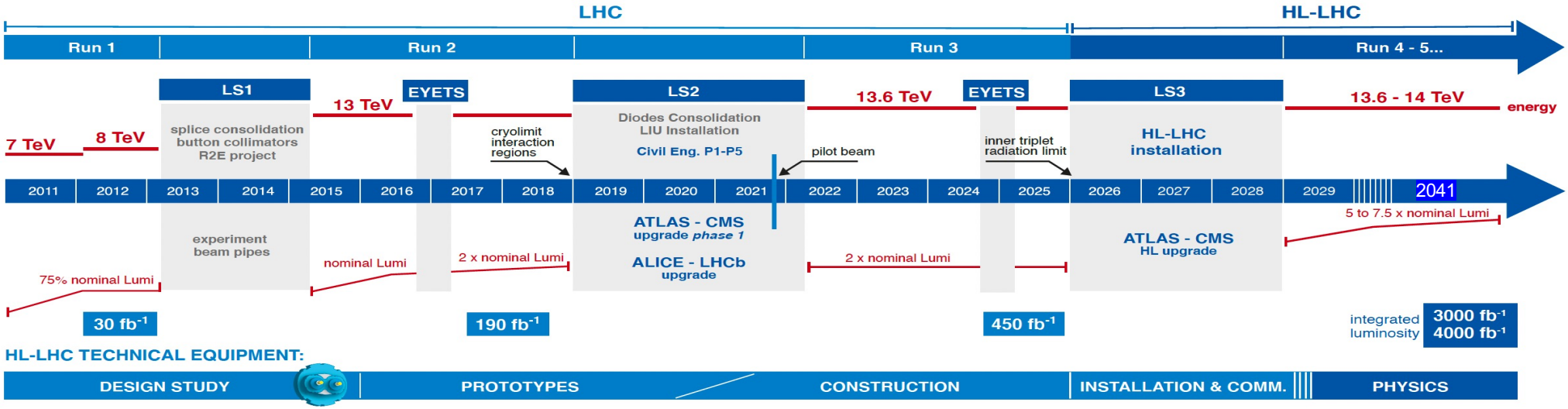
LHCP 2023, Belgrade

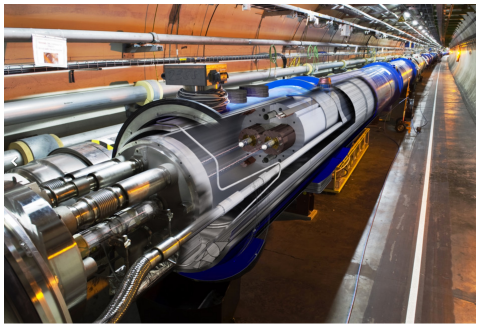
May 25, 2023

LHCPhysics
Belgrade, 22 - 26 May 2023

SLAC NATIONAL ACCELERATOR LABORATORY

LHC Timeline



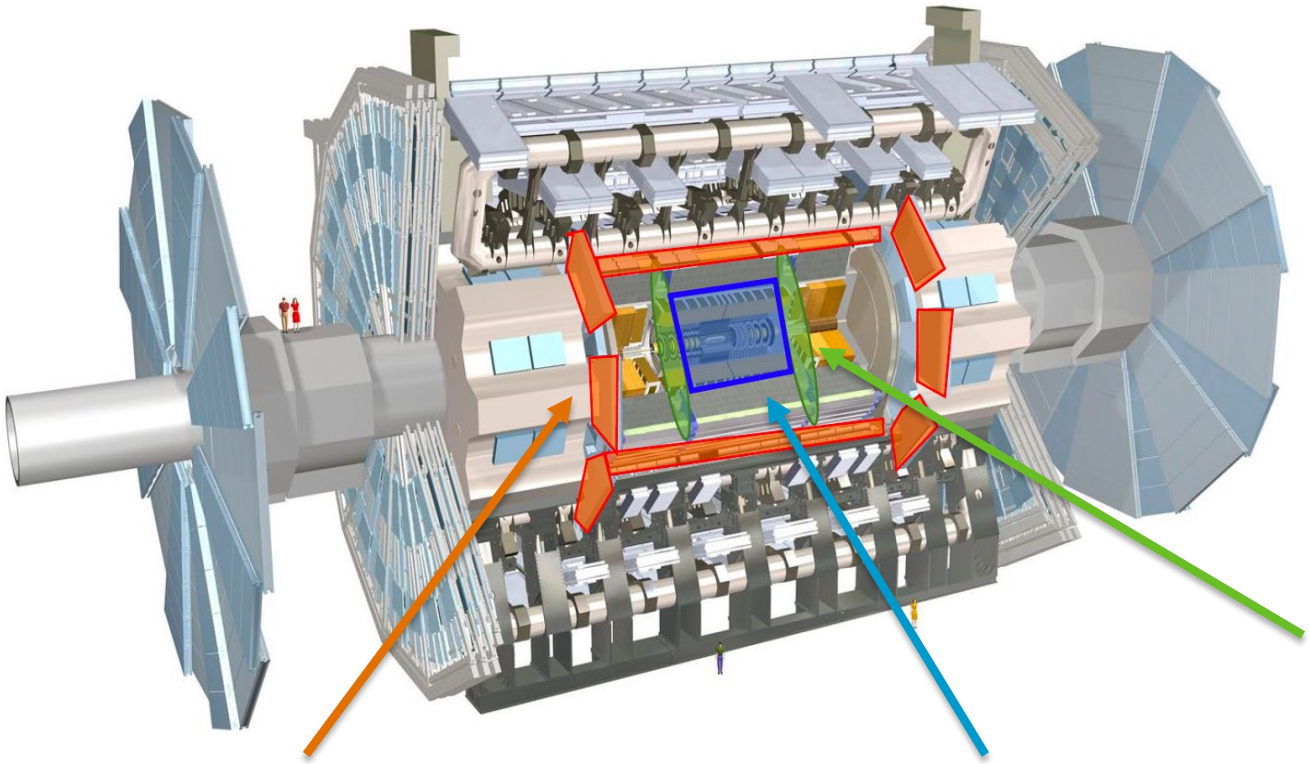


- High-Luminosity LHC (phase 2) to start in 2029 after LHC Long Shutdown 3 (LS3).
- Data taking until 2041, expected integrated luminosity of 3 ab^{-1}.
- Instantaneous luminosity to increase from $2 \cdot 10^{34}$ $s^{-1}cm^{-2}$ to $7.5 \cdot 10^{34}$ $s^{-1}cm^{-2}$.
- Peak leveled pile-up of up to 200 compared to 60 in the current run.

Major upgrades to the ATLAS detector are needed to cope with these requirements!

ATLAS Upgrade Overview

SLAC



Upgraded Trigger and Data Acquisition System

- Single Level Trigger with 1 MHz output
- Improved 10 kHZ Event Farm

Electronics Upgrades

- On-detector/off-detector electronics upgrades of LAr Calorimeter, Tile Calorimeter & Muon Detectors
- 40 MHz continuous readout with finer segmentation to trigger

High Granularity Timing Detector (HGTD)

- Precision time reconstruction (30 ps) with Low-Gain Avalanche Detectors (LGAD)
- Improved pile-up separation and bunch-by-bunch luminosity

New Muon Chambers

- Inner barrel region with new RPCs, sMDTs, and TGCs
- Improved trigger efficiency/momentum resolution, reduced fake rate

New Inner Tracking Detector (ITk)

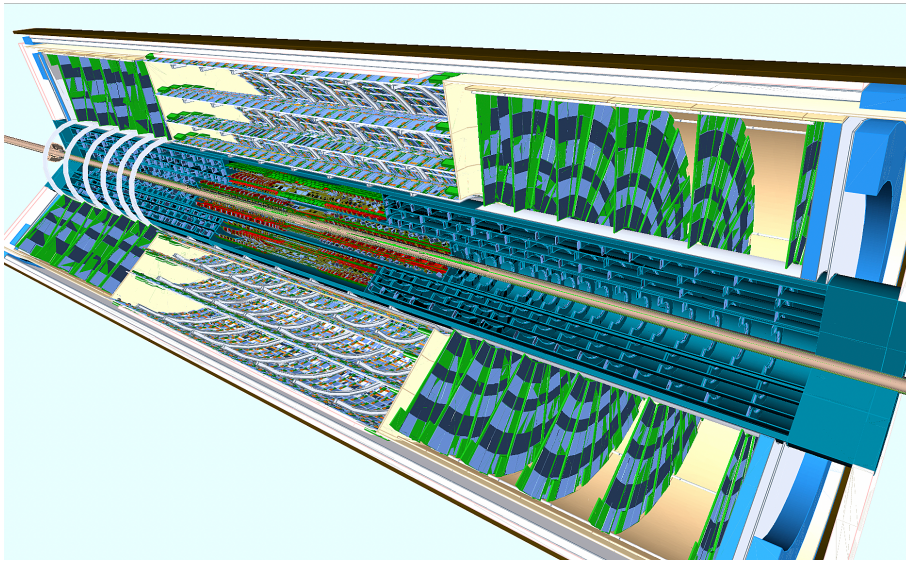
- All silicon with at least 9 layers up to $|\eta| = 4$
- Less material, finer segmentation

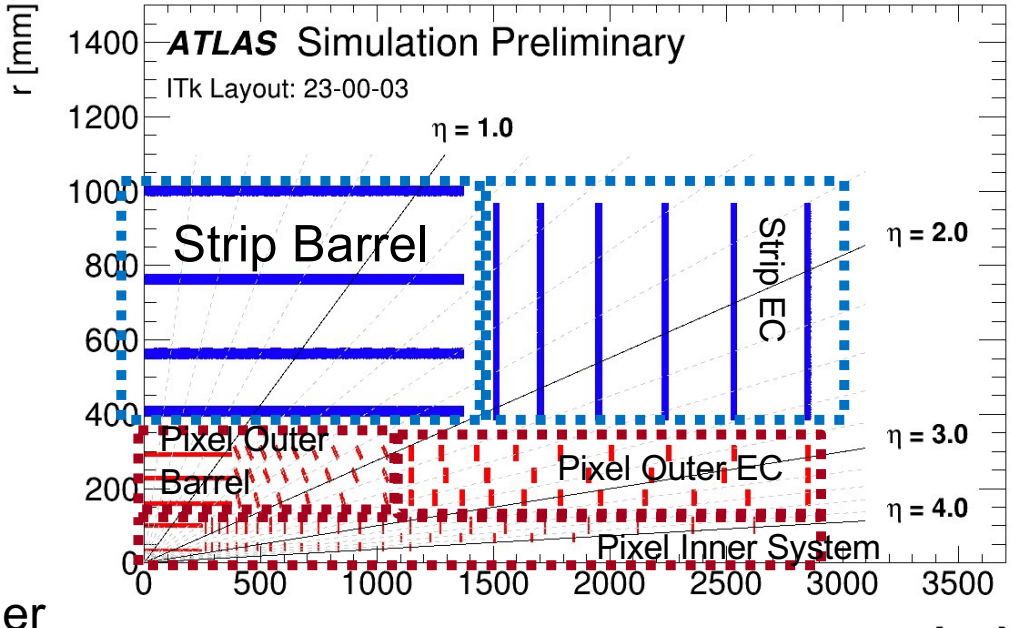
Additional small upgrades

- Luminosity detectors (1% precision)
- HL-ZDC (Heavy Ion physics)

Not covered in this talk.

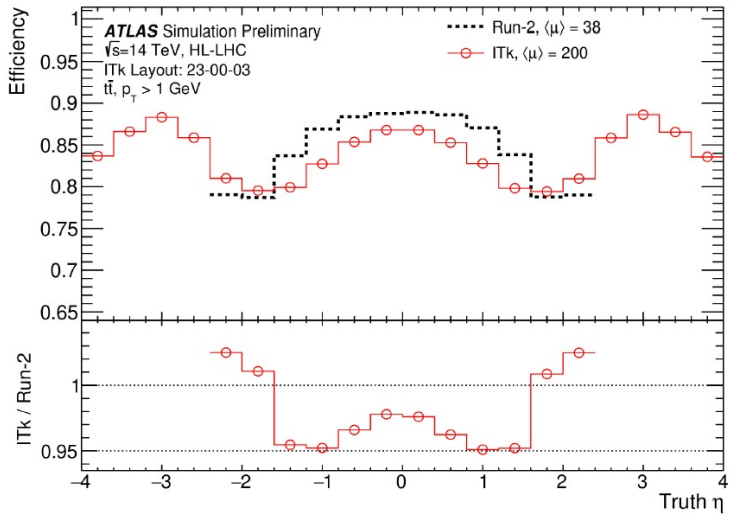
The Inner Tracker (ITk)





- Complete replacement of the current Inner Detector (Pixel, SCT, TRT).
- Silicon-only.
- Pixel (Inner system, outer barrel, outer endcap) and Strip detector (barrel, endcaps).
- 13 m^2 of silicon in Pixels, 168 m^2 in Strips.
- Eta coverage increase from 2.5 to 4.
- At least 9 silicon hits per track.
- Radiation tolerant up to 1 x 10^{16} n_{eq}/cm^2 (inner Pixels).

Tracking Efficiency
ITk vs. current ID



The ITk Pixel Detector

General features:

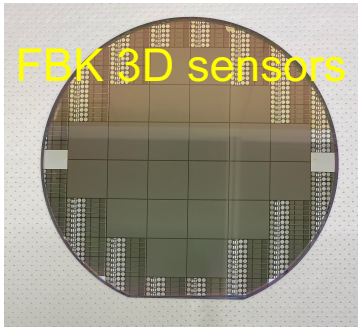
- Organized as three systems (inner, outer, outer endcaps).
- Five barrel-layers.
- More than 5,000,000,000 pixels.
- Inner system replaceable (radiation damage).
- Serial powering.

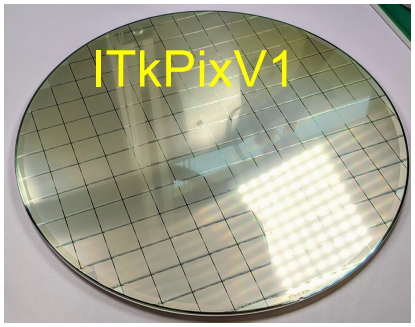
Sensors:

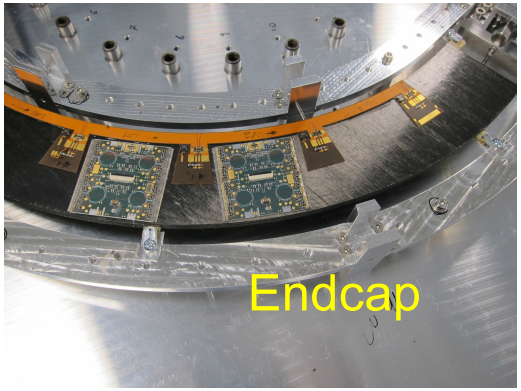
- Pixel sizes 25 x 100 μm^2 (innermost barrel) and 50 x 50 μm^2 (everywhere else).
- 3D sensors in innermost barrel/disks and planar sensors in the other layers.

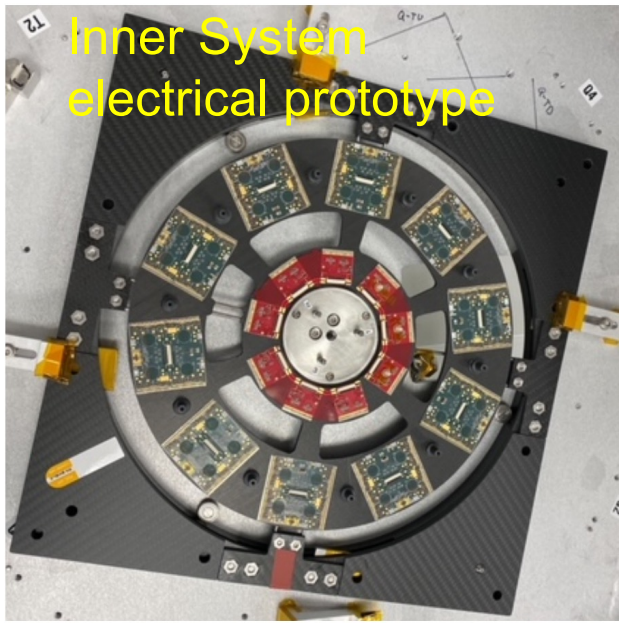
Production status:

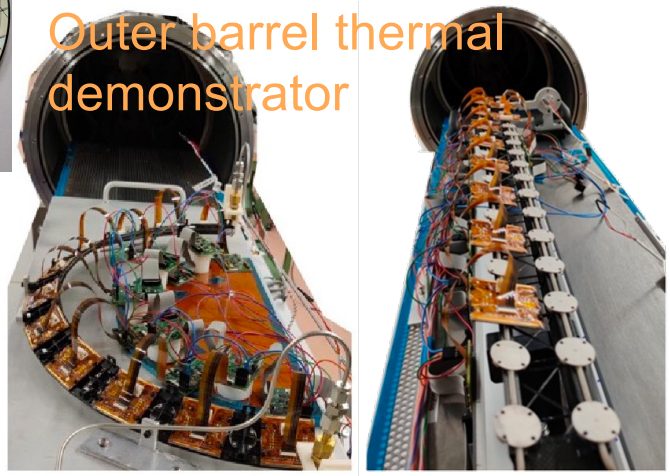
- All sensors are in pre-production.
- Hybridization of pre-production modules has started.
- ItkPixV2 readout chip has been submitted.







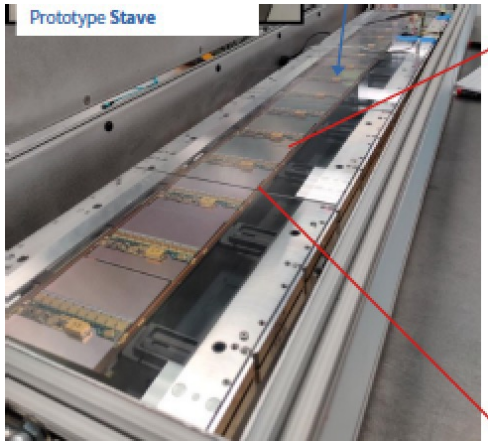


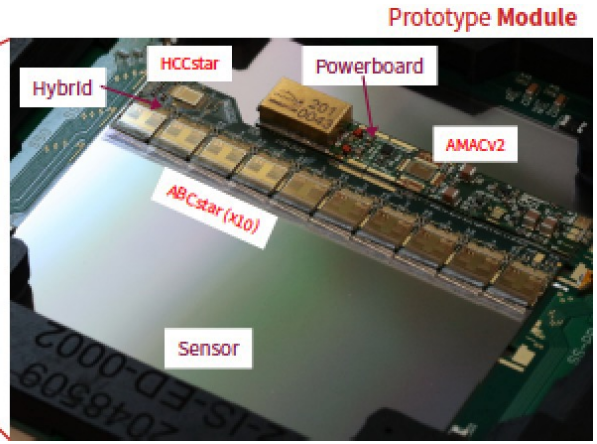


The ITk Strip Detector

General features:

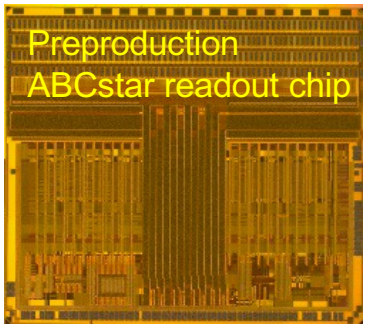
- Four-layer barrel and two six-disk endcaps.
- Angular coverage of $|\eta| < 2.7$.
- 18,000 modules.





Sensors/ASICs:

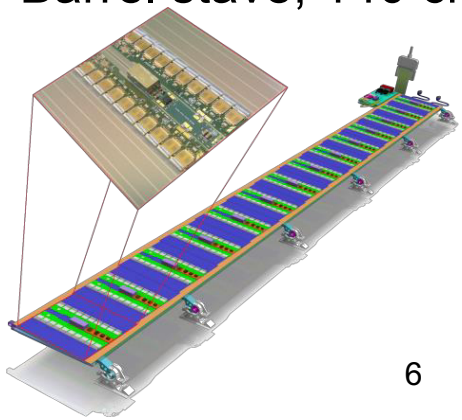
- Strip width ~75 μm.
- ~60 million channels.



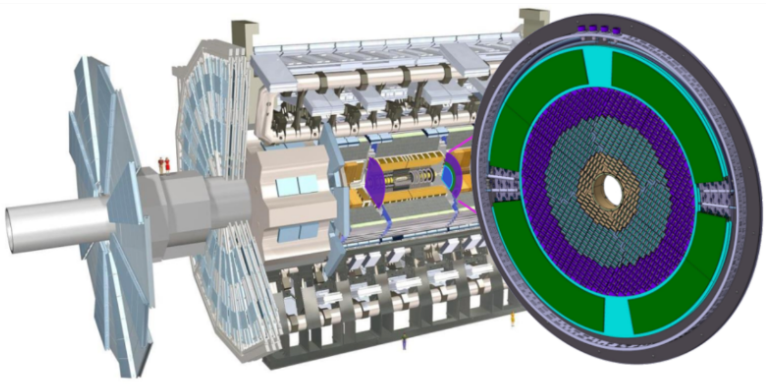
Production status:

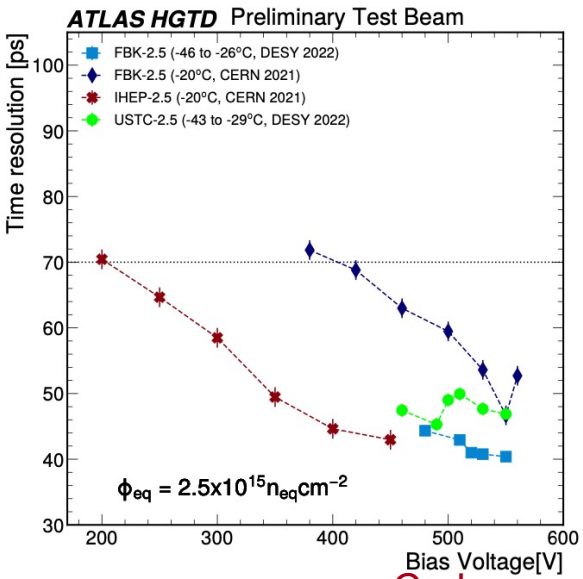
- Sensors: In production.
- ASICs: In production.
- Hybrids and modules in pre-production.
  Module pre-production impacted by cold noise issue. This is fixed now.

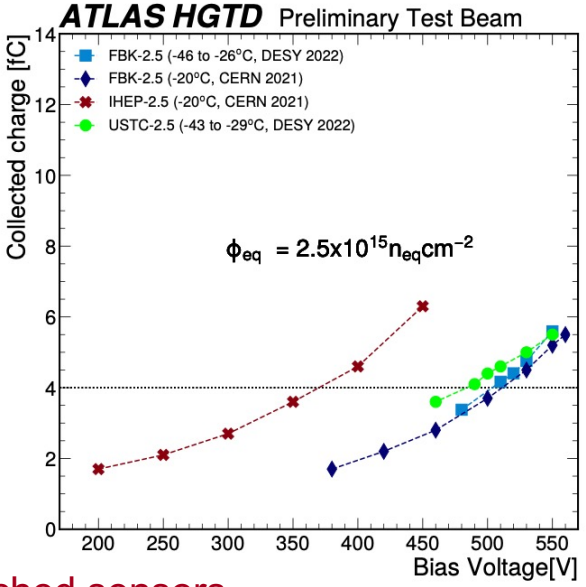
Barrel stave, 140 cm



High-Granularity Timing Detector (HGTD)

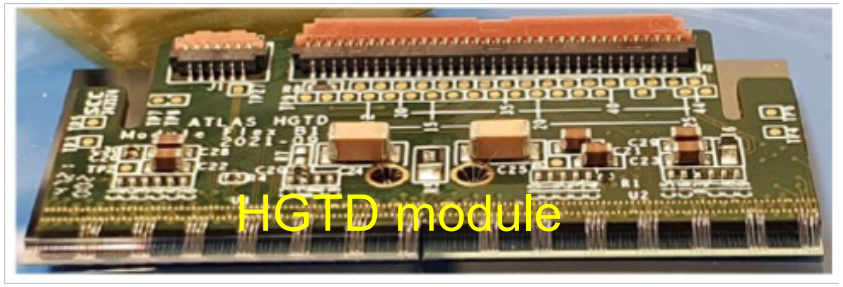






Carbon enriched sensors

- Completely new detector between ITk and endcap calorimeter to resolve pile-up through hit-timing information.
- $2.4 < \eta < 4.0$; Rmin= 12 cm; Rmax = 64 cm.
- Pixel size of 1.3 x 1.3 mm^2.
- Four layers of LGAD modules to achieve 30-50 ps resolution (70 ps per hit).
- Modules (2 ALTIROC frontends bump bonded on 2 sensors) have been demonstrated to work.
- Single-event burnout (SEB) was observed on LGAD sensors during testbeam. Mitigated by carbon-infused sensors with decreased high voltage.
- Altiroc3 readout chip was just received from TSMC.



Calorimeters

General

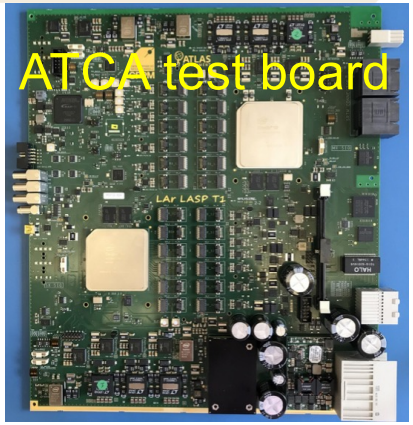
- New on-detector and off-detector electronics.
- Continuous readout at 40 MHz.

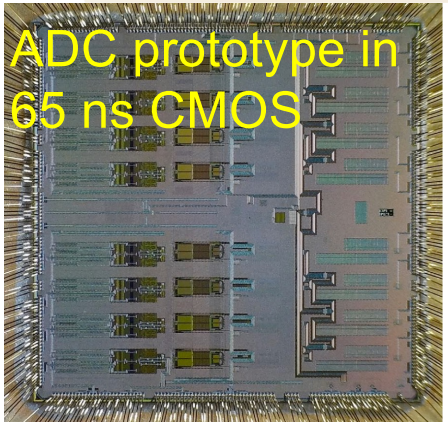
Liquid Argon Calorimeter (LAr)

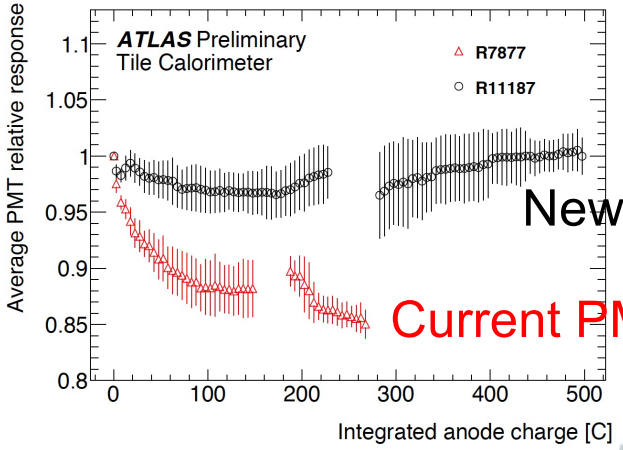
- Total bandwidth of 345 Tbps.
- New high precision frontend electronics (4 ASICS) with a 16-bit dynamic range and a linearity better than 0.1 %.
- ATCA boards for waveform feature extraction with ~33k links at 10 Gbps.

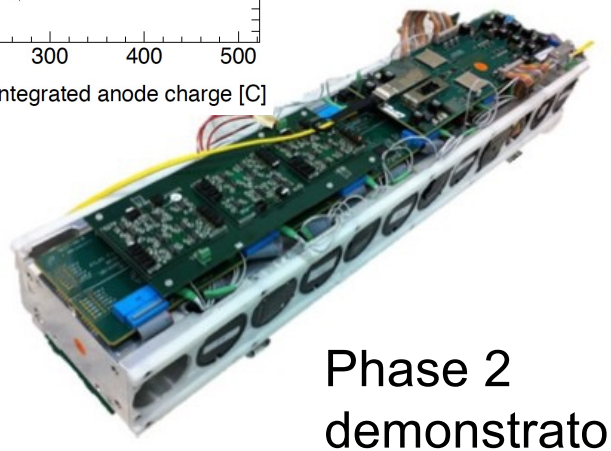
Tile Calorimeter:

- Replacement of the most exposed PMTs (about 10%).
- Replacement of passive PMT HV-dividers by active dividers for better response stability.
- On-detector electronics at advanced stage, main board production ongoing.
- Phase-2 demonstrator has been installed in ATLAS and is taking data.



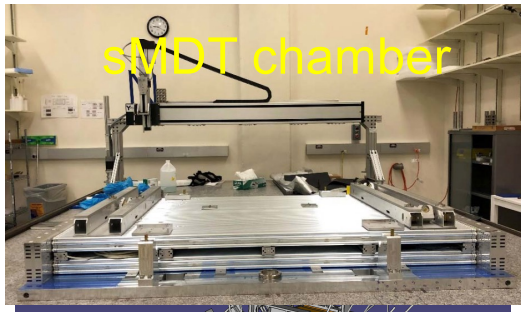


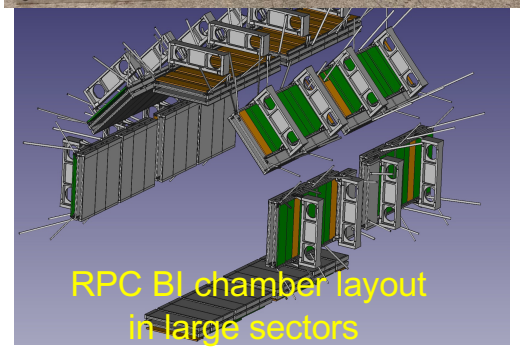


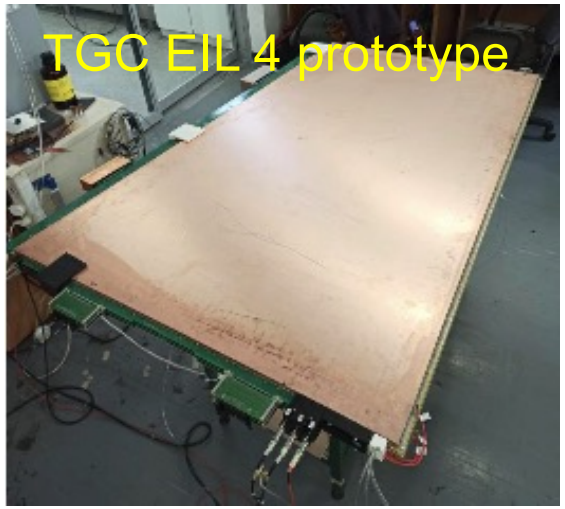


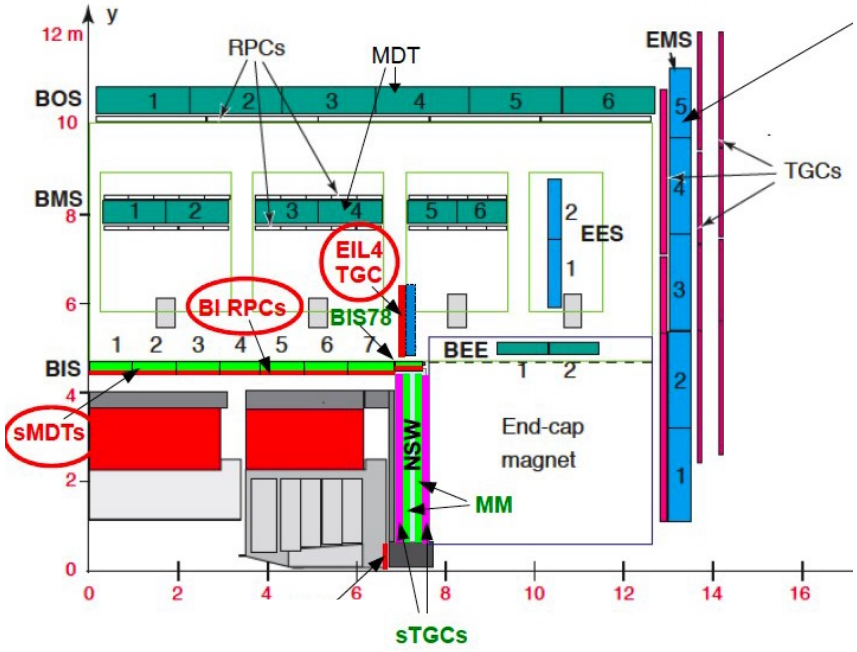
Phase 2 demonstrator

Muon Detectors





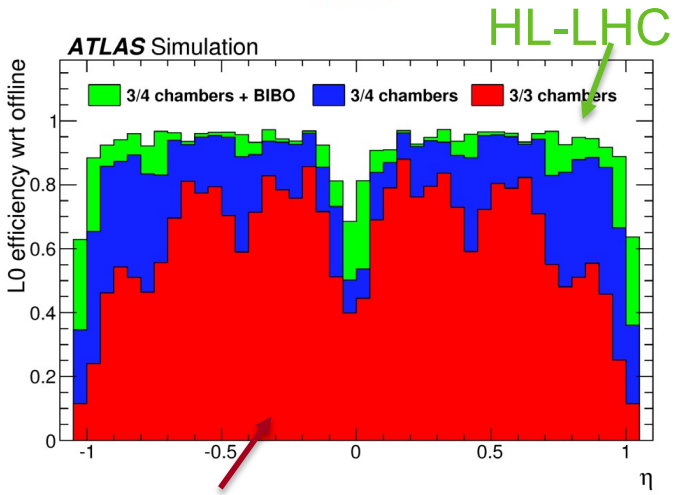




- Addition of layers of sMDT, TGC, RPC.
- MDT will provide L0 trigger information.
- Readout/trigger upgrade to send data at 40 MHz.
- Improved coverage, trigger uniformity, momentum resolution, fake rates.

Production status:

- **sMDT**: Chamber production far advanced, two thirds of the chambers already at CERN. Frontend-boards to be produced in the fall. Start of commissioning in early 2024.
- **RPC**: Second FE prototype delivery imminent. Prototype chambers extensively tested. ASIC engineering run in June.
- **TGC**: Design passed FDR, Completion of two preproduction modules imminent. FE ASIC production and QC completed.



Trigger and DAQ

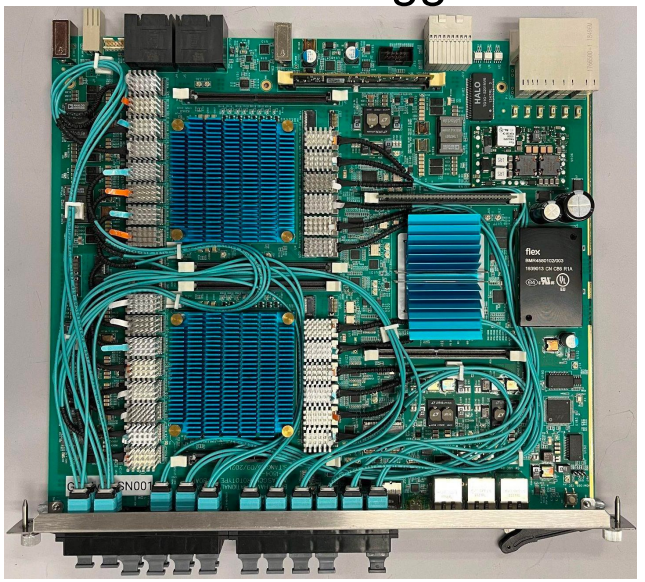
Trigger:

- Trigger data input at 40 MHz.
- Level-0: Rate 1 MHz, latency 10 μs.
- Level-3 / event building: Rate 10 kHz.
- Exploits full detector granularity and extended tracking range, improves muon trigger efficiency
- For the level-3 tracking, an associative memory solution has now been excluded. Instead, use COTS hardware. Either pure software solution, or GPU or FPGA card acceleration (under evaluation).

DAQ:

- Unified backend electronics based on custom PCIe FPGA cards (FELIX) instead of VME-based readout boards.

Level-0 Global Trigger Board



FELIX Prototype

Summary and Conclusion

To cope with the demanding conditions of HL-LHC, ATLAS will undergo a major upgrade in the next long shutdown (2026-2028).

- New detector components:
  - ITk, a new all-silicon tracker with an improved coverage up to $|\eta|<4$.
  - HGTD, an LGAD based timing detector
  - Additional sMDT, TGC, RPC muon chambers.
- Electronics upgrades:
  - LAr and Tile calorimeters and muon systems upgrading their frontend and backend electronics for the increased trigger and readout requirements.
- TDAQ upgrades:
  - Trigger system upgrade from 100 kHz to 1 MHz.
  - New readout boards for high bandwidth.

With these upgrades in place, ATLAS will be well prepared for many years of data taking at the high luminosity LHC!