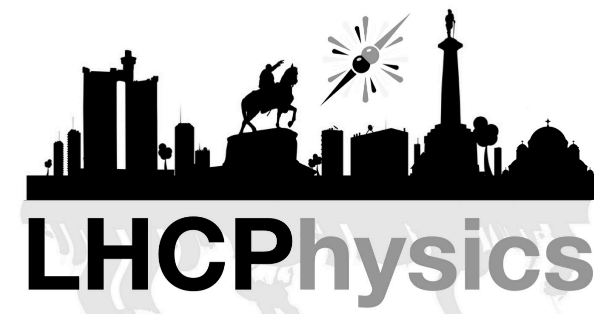
Future Monolithic Pixel Detectors in ALICE and beyond

Francesca Carnesecchi

On behalf of the ALICE collaboration



25th May 2023, Belgrade

CMOS MAPS – a short introduction

Qualitative timeline…

1969

Digital imaging → with the invention of the **C**harge-**C**oupled **D**evice (**CCD**) ,
→ Start of the the digital imaging **revolution**

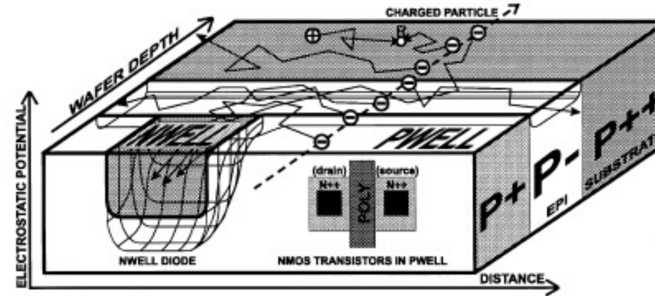
Nobel Prize in Physics in 2009
Willard S. Boyle and George E. Smith
"for the invention of an imaging semiconductor circuit - the CCD sensor"

Early 1990s

Emergence of **C**omplementary **M**etal-**O**xide **S**ilicon (**CMOS**) Image Sensor technology

Since 15 years → leading imaging technology

2001



MIMOSA-1 Early versions with thin and **low resistivity** epi-layer
https://doi.org/10.1016/S0168-9002(00)00893-7

- Shallow depletion region → low charge collection efficiency
- Detector element covers only a small fraction of the pixel area

Today

CMOS used in **camera phones**, vehicles, machine vision, human recognition and security systems
- most widespread implementation of image sensors, advantage → price
- CMOS Imaging Sensor (CIS) capacity is extending to 28-22nm

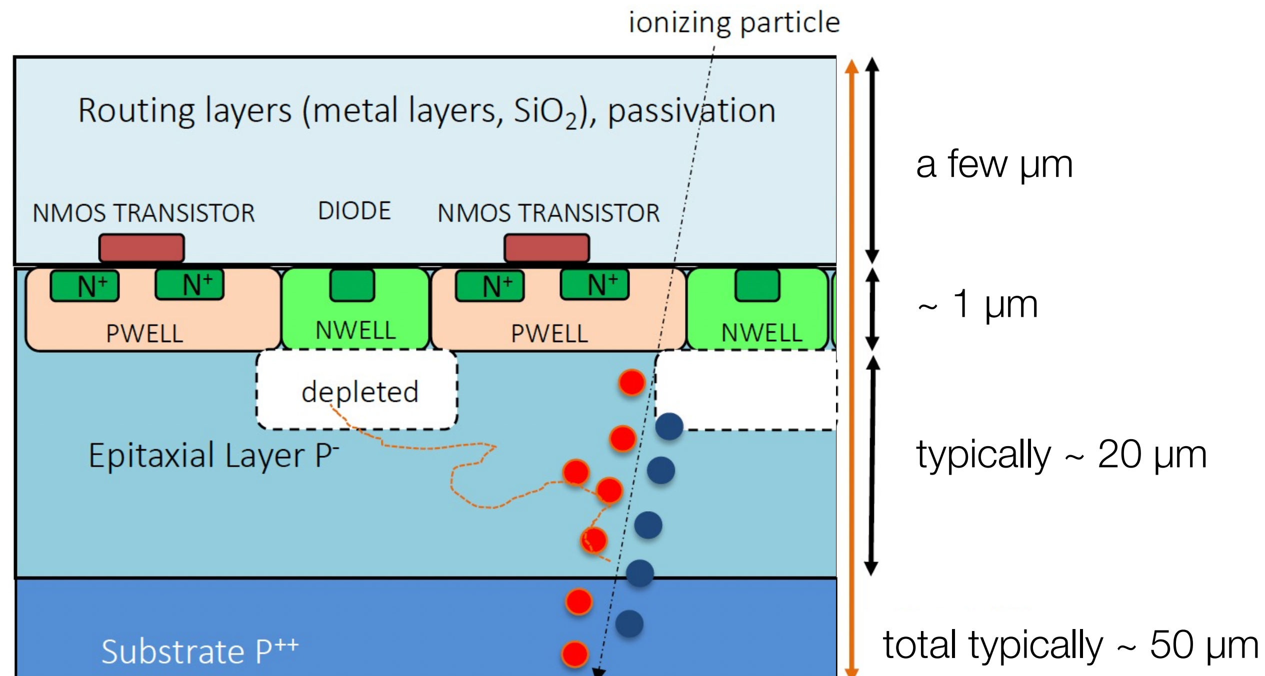
Big steps for **charge particles detection**

CMOS MAPS – evolution for charged particles

Recipe's evolution for CMOS MAPS for charged particles…

- CMOS on low-resistivity silicon
- high resistive epitaxial layer

In order to properly detect charged particles → **high resistive epitaxial layer**, with doping few order of magnitude smaller than one of the p++ substrate



Epitaxial layer partially depleted
Minority carriers **diffuse** in the epi layer…

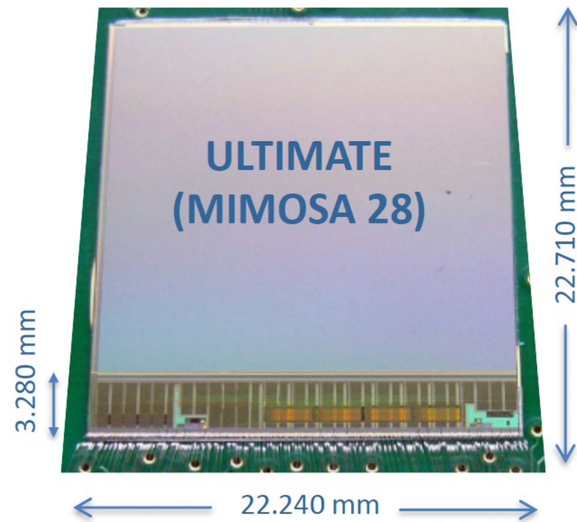
…potential barriers at its boundaries which keep minority carriers confined in epi…

… till they reach the depleted region → **drift**

N.B. **NMOS transistors in a pwell** → to shield the source and drain junctions from the epitaxial layer
→ **essential**, otherwise these sources and drains would act as collection electrodes
→ would prevent the nwell from collecting all the signal charge.

STAR – first application in HEP

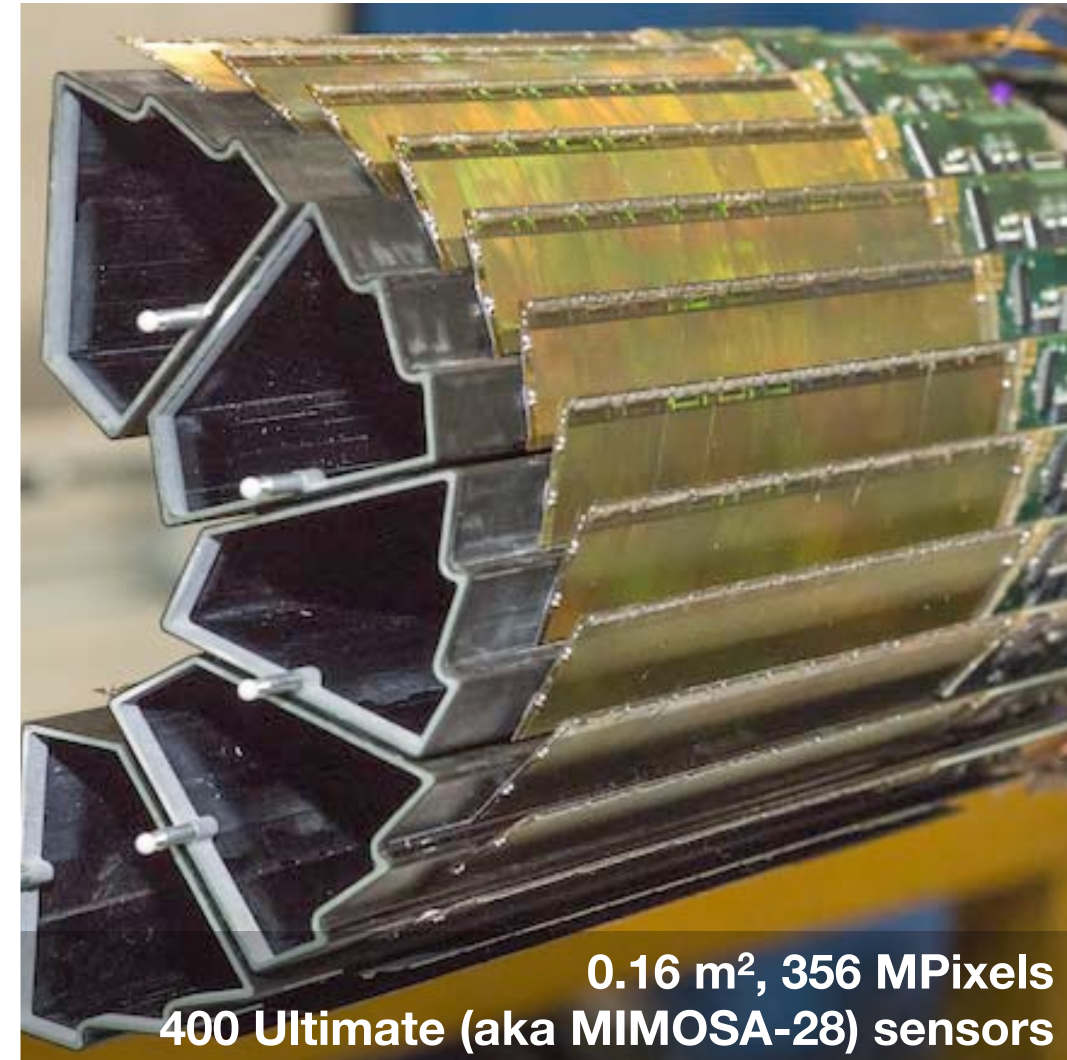
Full detector in 2014



MIMOSA-28
high-resistivity p-epi layer
The STAR building block

- x/X_0 = **0.39%** (first layer at 28 mm)
- technology node **0.35 µm CMOS**
- power **~ 150 mW/cm²**
- 18.4 µm pitch
- 20 µm not fully depleted and no reverse bias
  - Charge collected (mostly) by diffusion
  - **NIEL** up to ~10^{12} 1MeV n_{eq}/cm^2
- **in-pixel simple circuit**: 3T structure

Physics Runs in 2015-2016



CMOS MAPS – INMAPS process

Recipe's evolution for CMOS MAPS for charged particles…

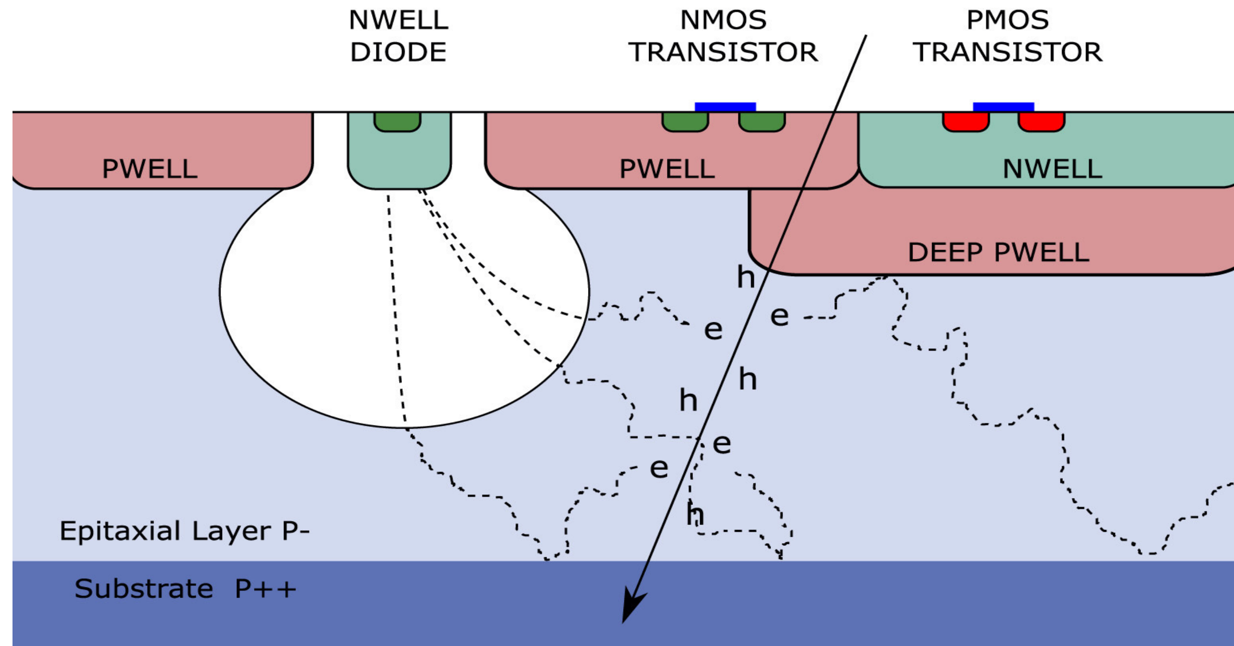
CMOS on low-resistivity silicon

high resistive epitaxial layer

INMAPS process

2008, https://doi.org/10.3390/s8095336

STFC development, in collaboration with TowerJazz



Additional **deep P-well** :

- no charge collection competition between diode and N-well
- CMOS electronics in pixel
- faster

Before

limitation of in-pixel circuitry (only NMOS)

Now

new generation of CMOS APS for scientific applications with **complex CMOS circuitry inside the pixel**

ALPIDE in ALICE – ITS2

First MAPS in HEP with complex sparse readout similar to hybrid sensors

Inner Tracking System 2 (ITS2) upgrade – installation during 2021 (LS2)

ITS2: total of 7 layers, 10 m², 24k chips, 12.5 Giga-Pixels

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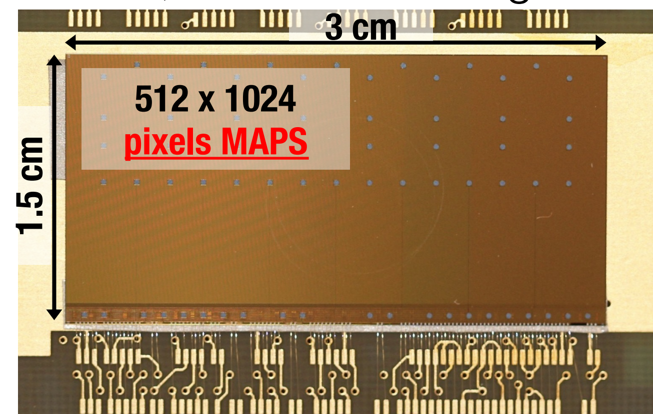
ALPIDE, the ITS2 building block



- **TJ CMOS 180 nm**, high-res. p-type epi layer (25μm)
- Small n-well diode (2μm) → low capacitance (~fF)
- **INMAPS**
- Reverse bias voltage
- pixel size ~ 27x29 μm^2
- **NIEL**~2.7 10^{13} 1 MeV n_{eq}/cm^2
- 30 nW /pixel (**<50 mW/cm²**)
- 23 mm from IP
- **0.36%** x/X_0/layer, IB

ALPIDEs used also by **M**uon **F**orward **T**racker in ALICE and in **sPHENIX** with a clone of the **I**nner **B**arrel

ALPIDE in ALICE – ITS2

Currently taking data in ALICE (since 2 years):

- with stable operation of all the 24k ALPIDEs
- >99% functional pixels
- very low FHR < 10^{-7} hits/(events pixel)

→ state of art for CMOS MAPS application in HEP

More about ITS2 performances in **"Run 3 Performance of new hardware in ALICE"**, **J. Liu, 23/05 11:30**

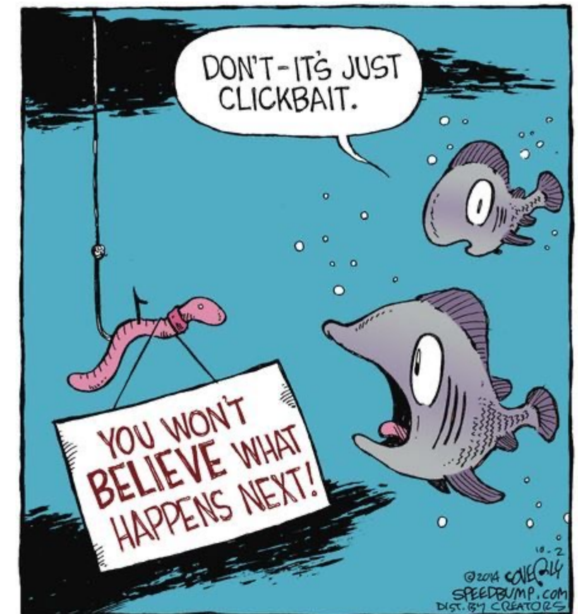
What next?
What do we need further in HEP?

Improve:

- **radiation hardness**
- **position resolution**
- **material budget**
- **power consumption**
- scalability (larger and **larger areas**)

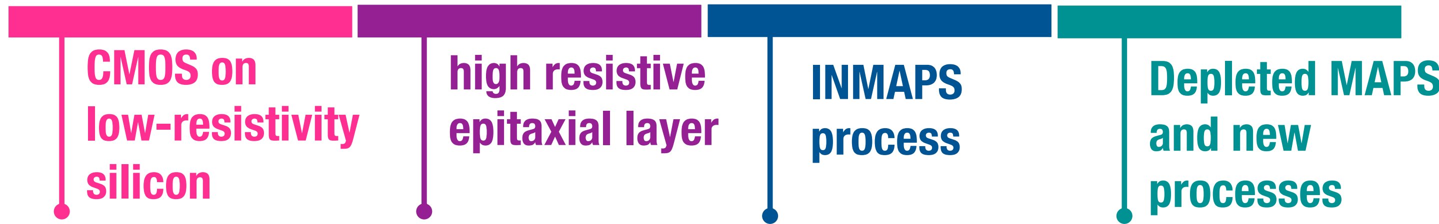
How:

- pixel pitch ~10-20 µm
  - also linked to **deeper sub micron tech. node** → 65 nm node
- **larger wafers**: 200 mm (8”) → to 300 mm (12”)
- **stitching**
- …

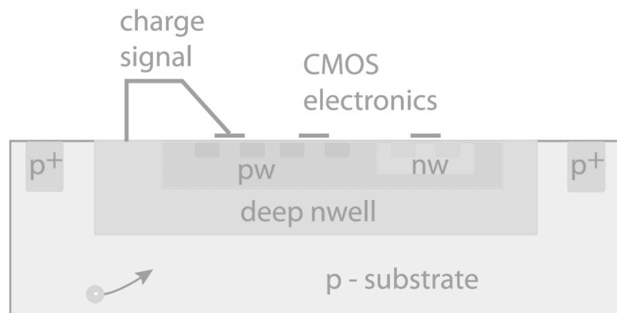


CMOS MAPS – Fully depleted, small electrode

Recipe's evolution for CMOS MAPS for charged particles…



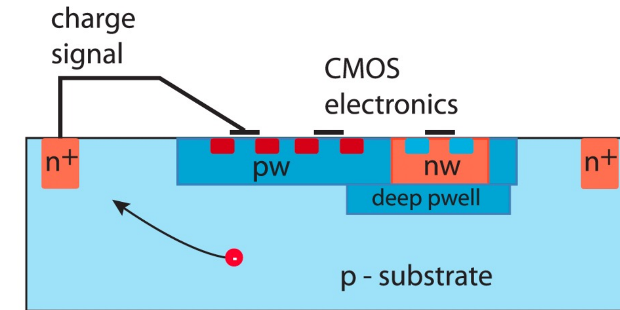
A common path in order **to improve the radiation hardness** and the time resolution → **fully depleted CMOS MAPS**



Electronics inside charge collection well

large collection electrode

- → C~300 fF → higher noise O(100 e-) and speed/power penalty
- high and homogeneus electric field
- Large depletion depth
- less trapping -> **radiation hard**
- possible cross-talk (digital to sensor)



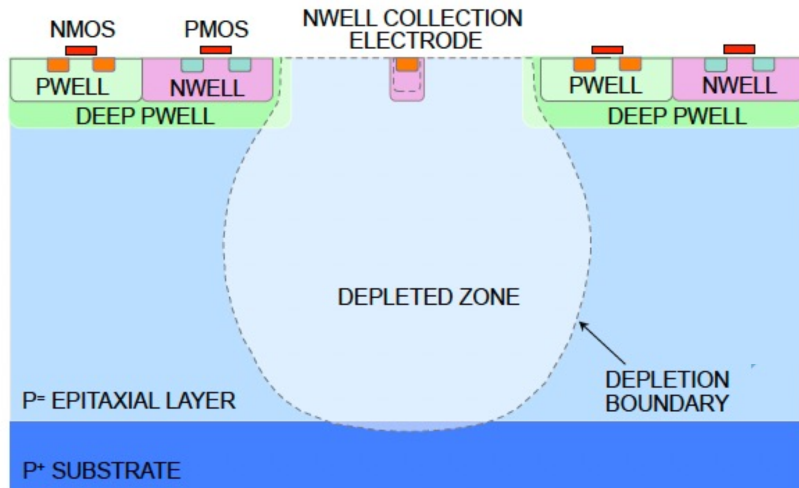
Electronics outside charge collection well

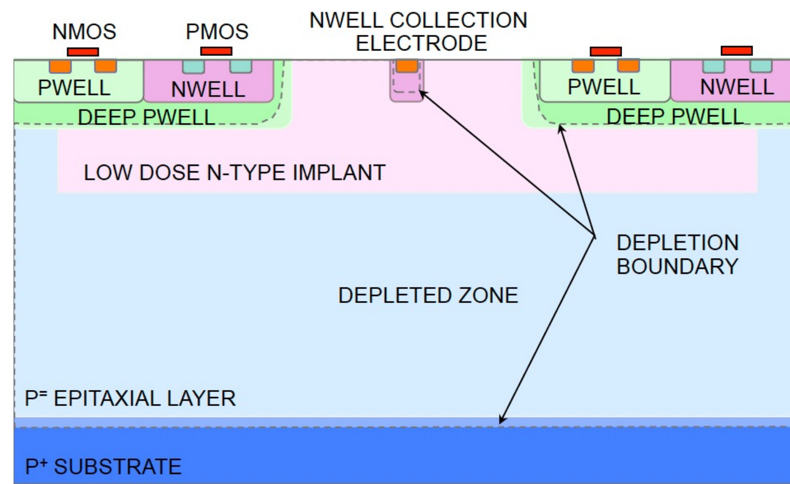
small collection electrode

- → C~3fF → reduced noise O(10 e-) and lower analogue power budget (noise, speed)
- potentially low field regions
- smaller depletion depth, **needs process modification**
- radiation hardness **needs process modification**
- less prone to cross-talk

CMOS MAPS – Fully depleted, small electrode

process modification





https://dx.doi.org/10.1016/j.nima.2017.07.046
https://doi.org/10.22323/1.420.0083

Standard ALICE ITS2 type

- partially depleted epi layer
- Partially collected by diffusion → collection time ~30 ns
- Operation up to 2 10^{13} n_{eq}/cm^2

Modified with gap planar junction (N-implant) separate from the collection electrode with gap in the low dose n-type implant

- **more volume can be depleted**
- Fully operational up to 10^{15} n_{eq}/cm^2
- better charge collection in lateral direction

→ Excellent co-operation with foundry

R&D started already by ALICE and followed by MALTA, CLICpix, FastPix

Charge sharing

Charge Collection efficiency and speed

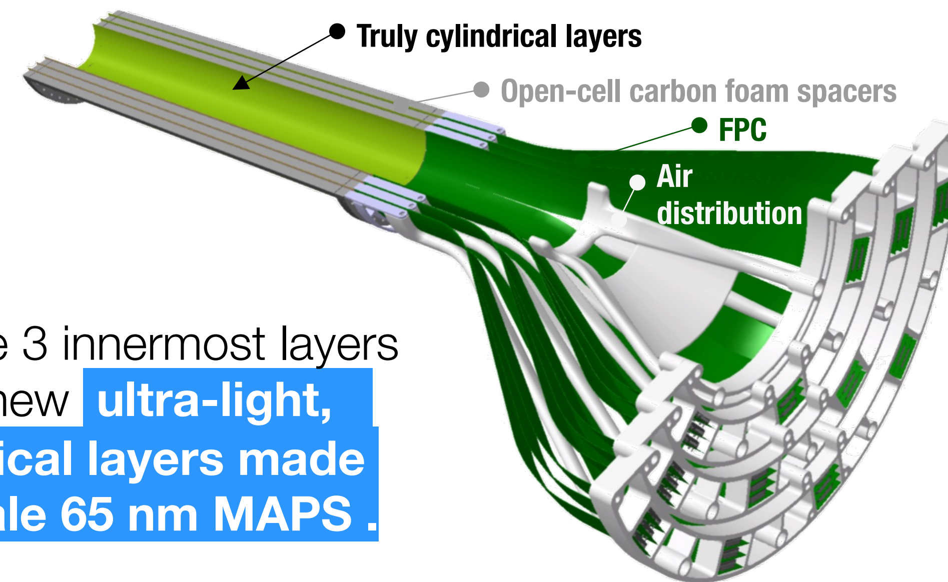
ALICE applications – ITS3

More about ITS3 performances and physics motivations in **"ALICE upgrades"**, **R. H. Munzer, 25/05 17:24**

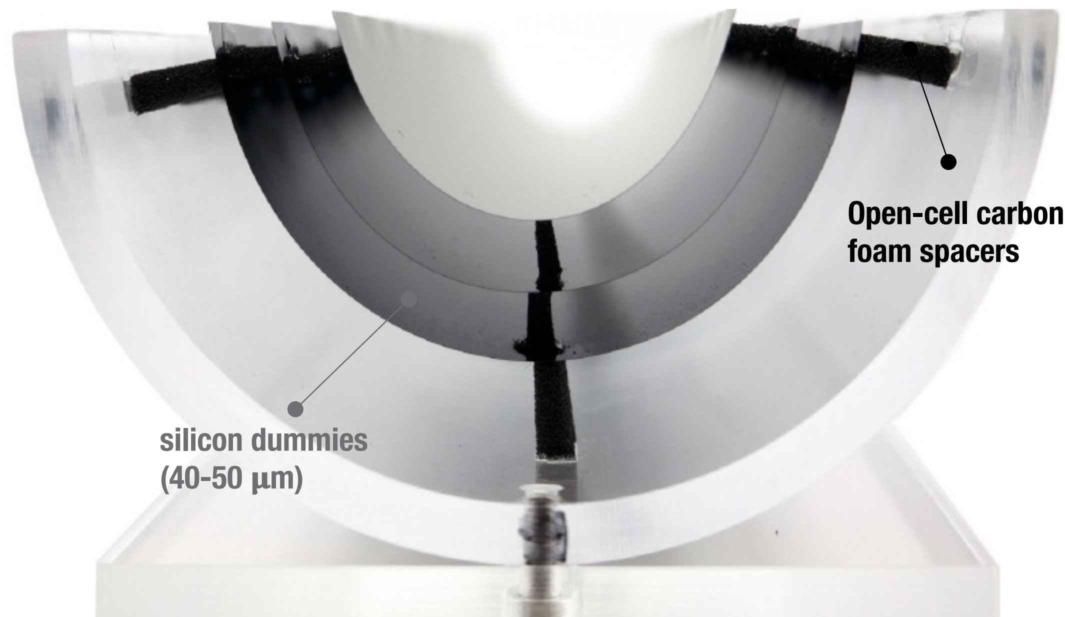
LHC LS3, 2027/28

2023	2024	2025	2026	2027	2028	2029	2030	2031	2032
RUN 3			LS3			RUN 4			

ITS2 → ITS3



Replacing the 3 innermost layers of ITS2 with new **ultra-light, truly cylindrical layers made of wafer scale 65 nm MAPS .**



From 432 to 6 bent sensors

- 300 mm **wafer-scale** MAPS sensors, fabricated using **stitching**
- **bent** to the target radii (L0 23 mm → 18 mm, closer to the interaction point thanks to the new beampipe at 16 mm)
- mechanically held in place by carbon foam ribs
- cooled down by air
- **0.02-0.05% X_0**

N.B. Other experiments even beyond LHC already shown interest in this development
→ **ITS3 R&D will pave the way for an ultimate vertex detector concept**

ALICE applications – ITS3

More about ITS3 performances and physics motivations in **"ALICE upgrades", R. H. Munzer, 25/05 17:24**

LHC LS3, 2027/28

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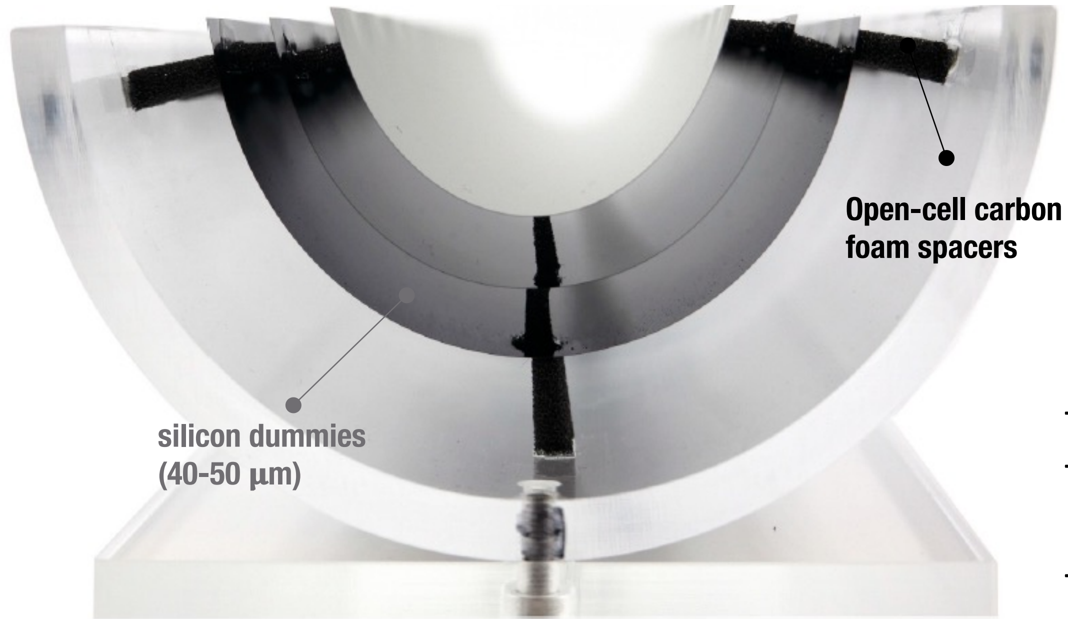
ITS2 → ITS3



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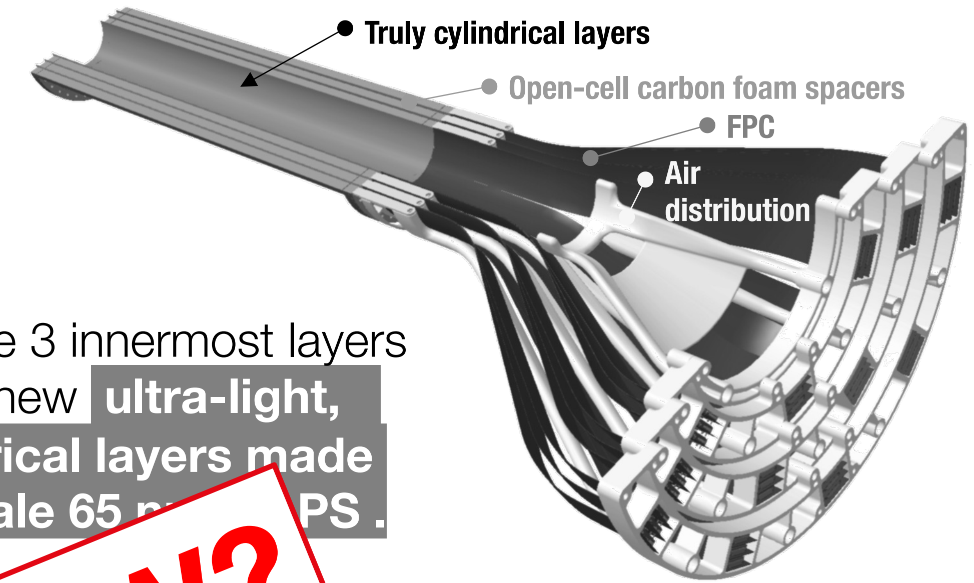

Replacing the 3 innermost layers of ITS2 with new **ultra-light, truly cylindrical layers made of wafer scale 65 n... ...PS .**

HOW?

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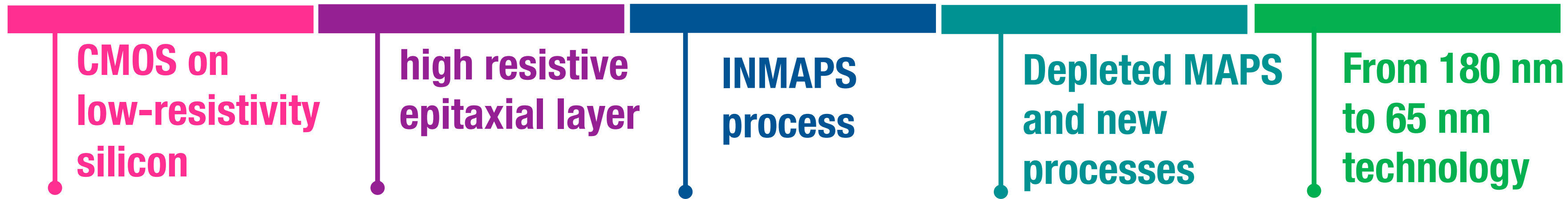
CMOS MAPS – 65 nm

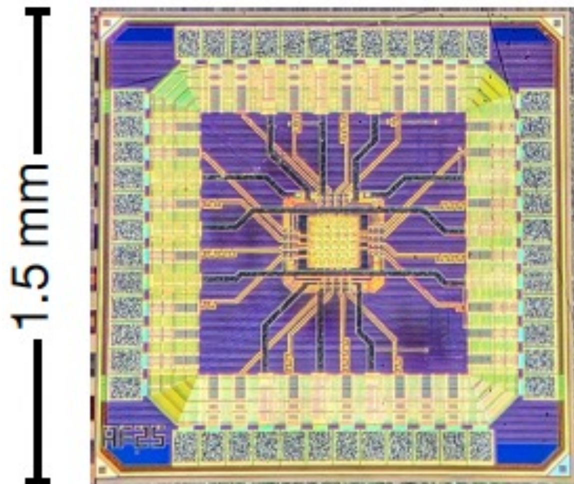


First submission in the Tower Partners Semiconductor **(TPSCo) 65 nm technology**

Verification of the technology for charge collection efficiency, detection efficiency, radiation hardness:

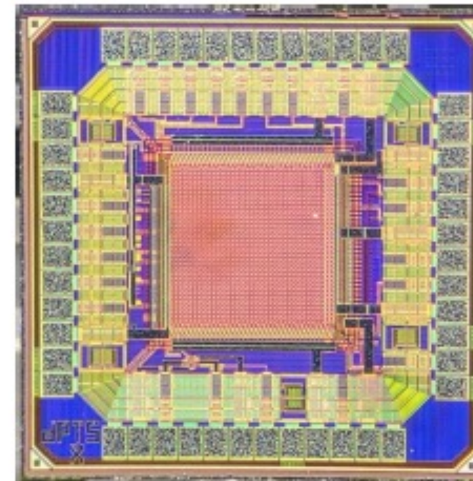
- larger wafers: 300 mm (instead of 200 mm), single "chip" is enough to equip an ITS3 half-layer
- smaller feature sizes to: lower power consumption, increase spatial resolutions, increase in-pixel circuitry

APTS



- **matrix**: 6x6 pixels
- **readout**: direct **analogue** readout of central 4x4
- **pitch**: 10, 15, 20, 25 μm
- **process**: 3 variants

DPTS

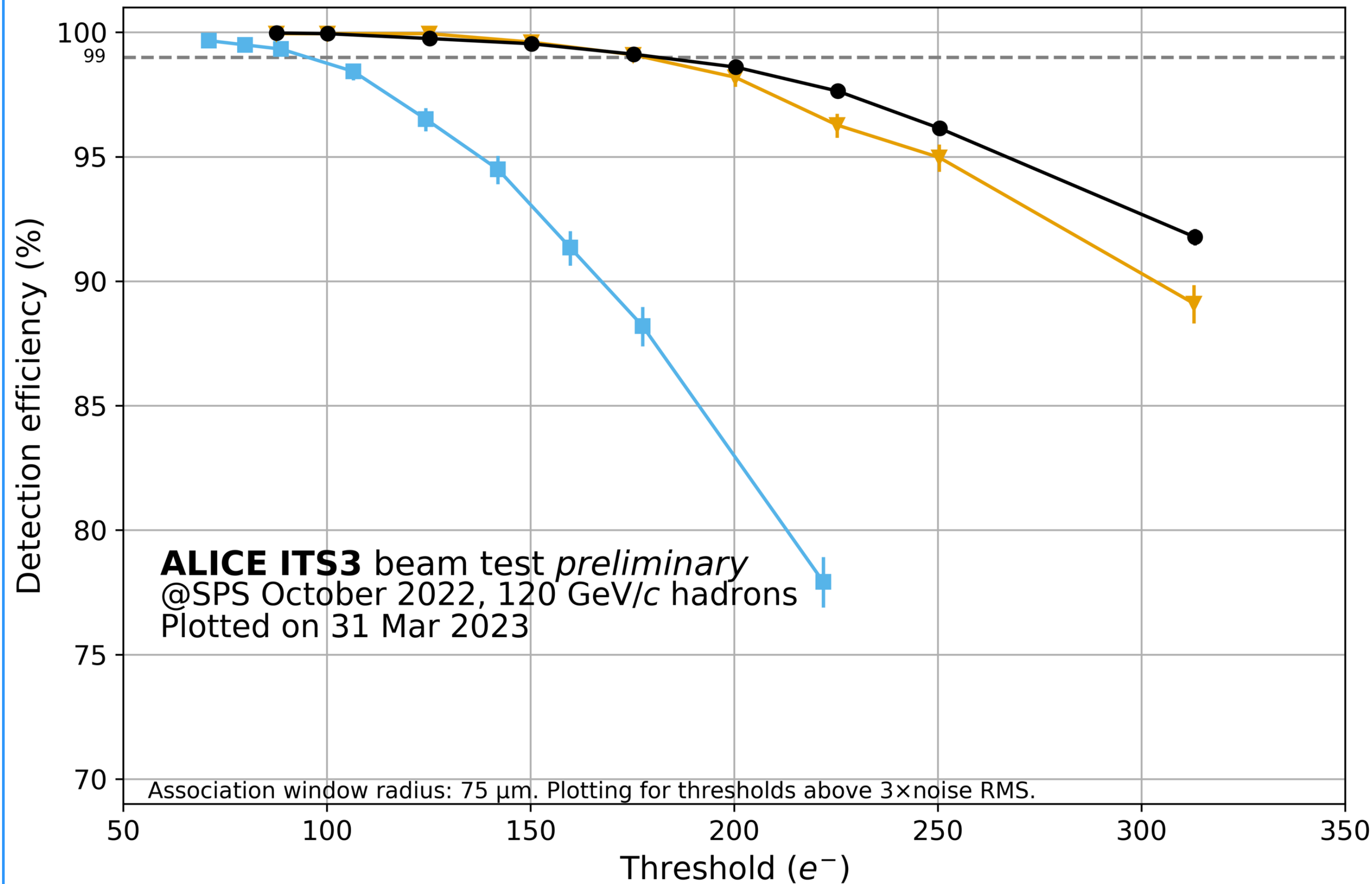


- **matrix**: 32x32 pixels
- **readout**: async. **digital** with ToT
- **pitch**: 15 μm
- **process**: 1 variant

CMOS MAPS – 65 nm

- Excellent detection efficiency over large threshold range for modified processes

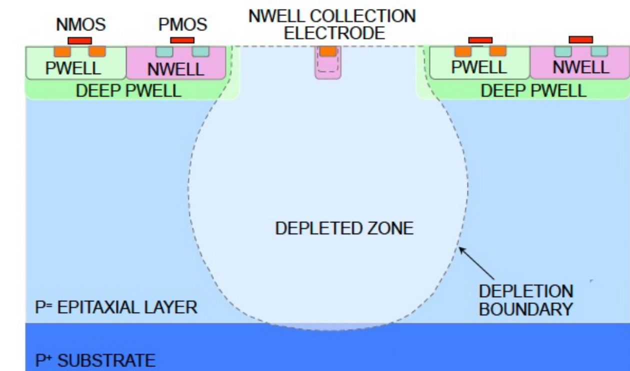
Beam test results



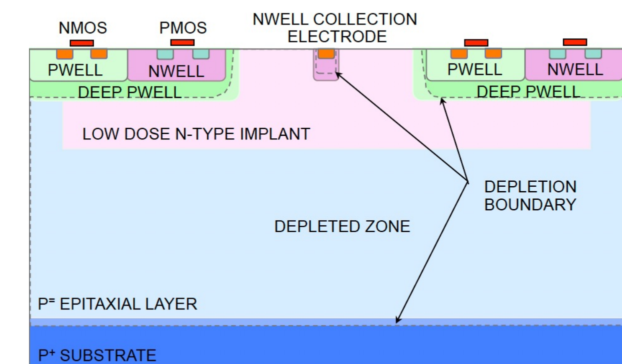
APTS SF
Non-irradiated
pitch: 15 µm
split: 4
I_{reset} = 100 pA
I_{biasn} = 5 µA
I_{biasp} = 0.5 µA
I_{bias4} = 150 µA
I_{bias3} = 200 µA
V_{reset} = 500 mV
V_{pwell} = V_{sub}=-1.2 V
T = 20 °C

Standard
Modified
Modified with gap

Standard



Modified with gap



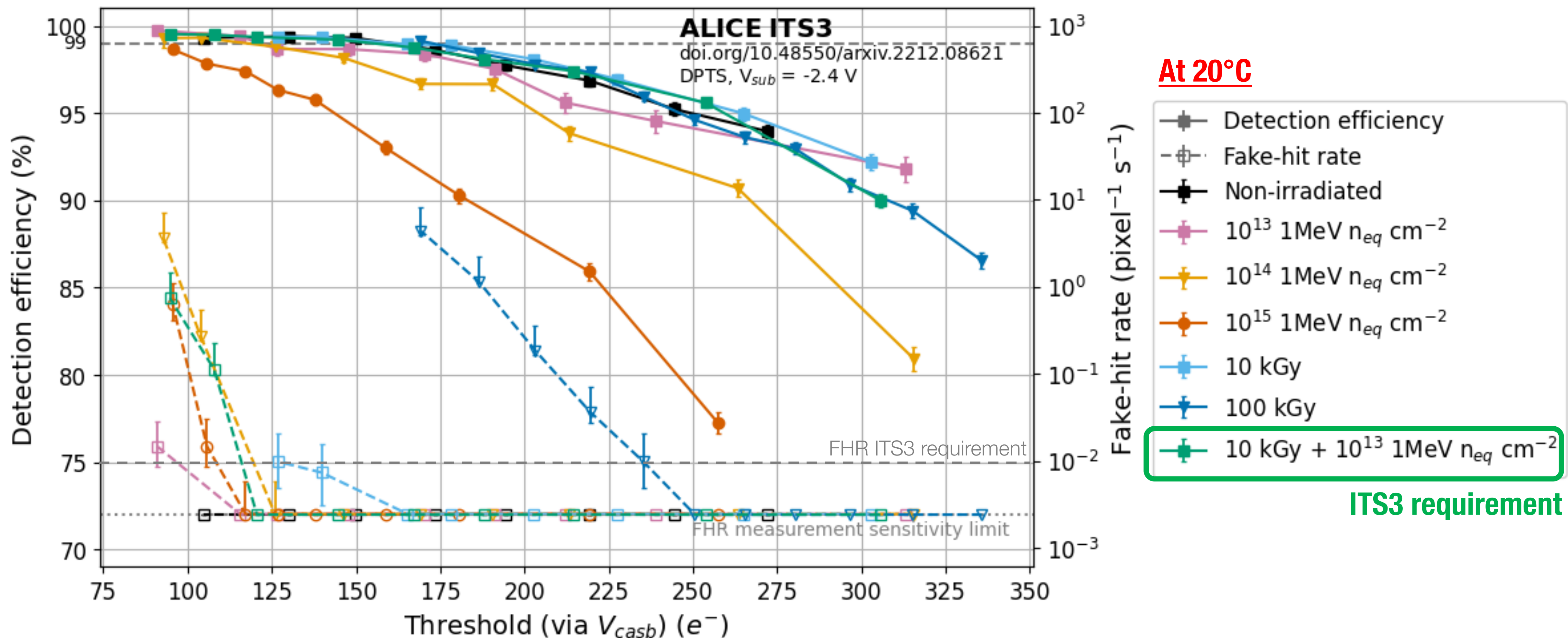
CMOS MAPS – 65 nm

https://arxiv.org/abs/2212.08621

Process: modified with gap

- At ALICE-ITS3 requirements **irradiation** level slightly larger fake rates, but **still largely operational**
- At **10^{15} n_{eq}/cm^2** → **~99% efficiency** reached **at 20°C**

Beam test results



CMOS MAPS – Silicon flexibility and bending

Recipe's evolution for CMOS MAPS for charged particles…

- CMOS on low-resistivity silicon
- high resistive epitaxial layer
- INMAPS process
- Depleted MAPS and new processes
- From 180 nm to 65 nm technology
- Silicon flexibility and bending MAPS

- Dummy wafer of 50 um can be wrapped around beam pipe
- Bending force scales as $(\text{thickness})^{-3}$
- Radii of 1.8 cm are easily reached

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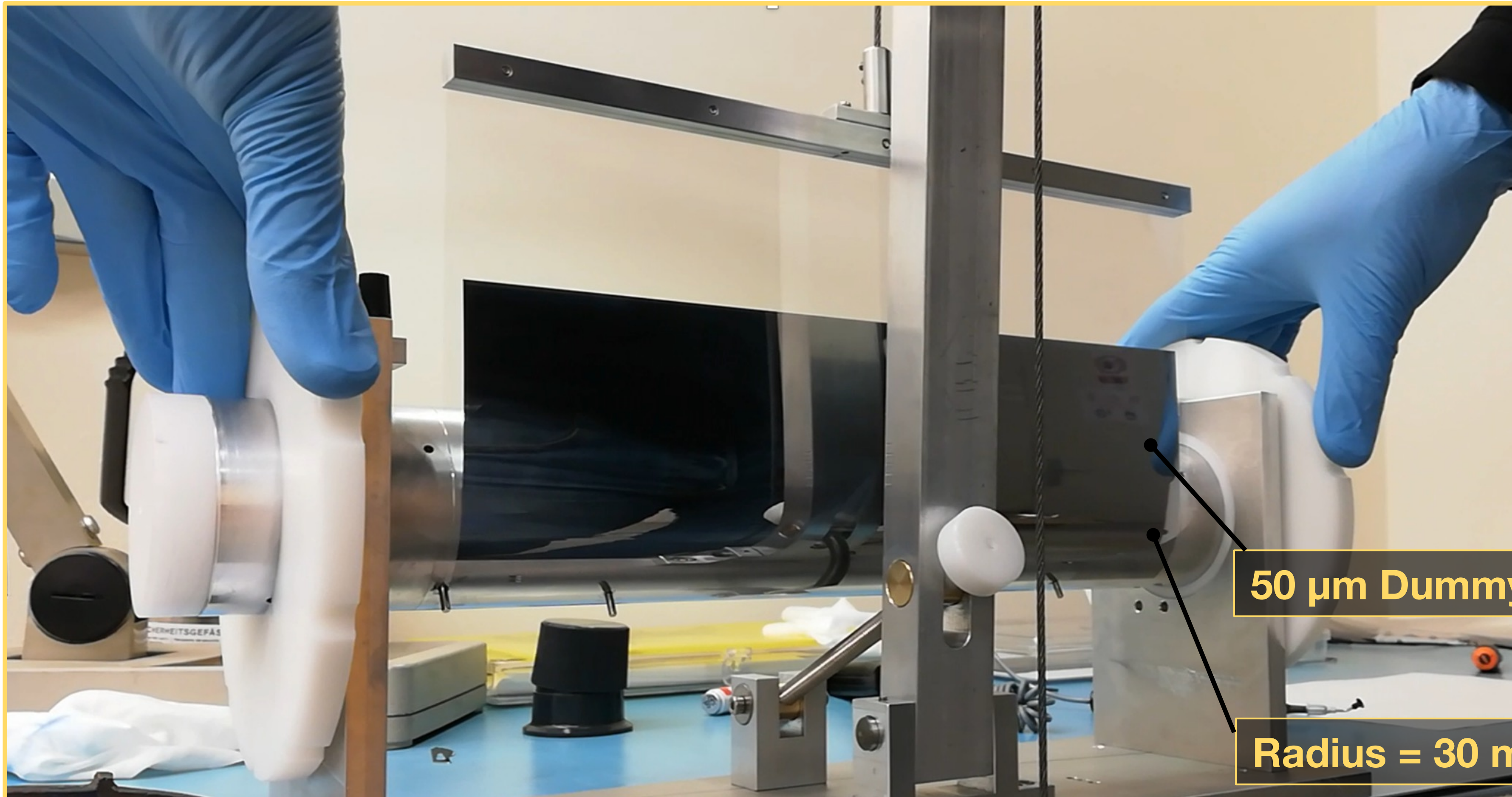

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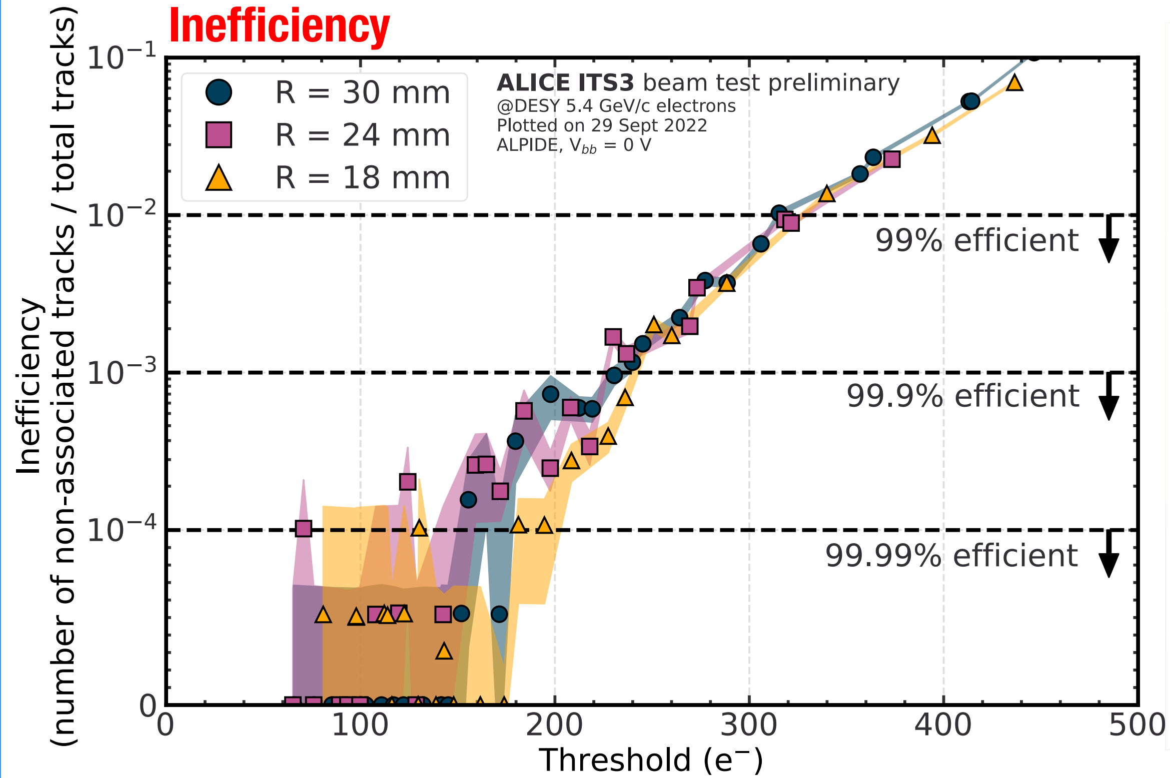
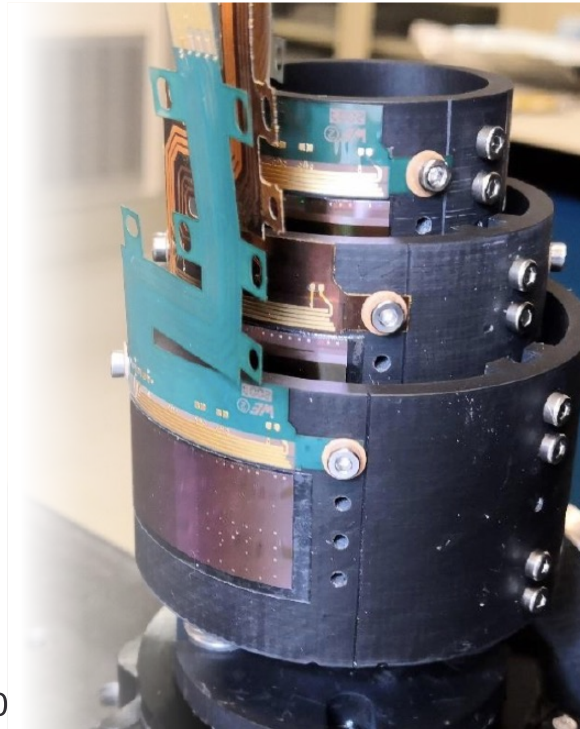
Bending of 180 and 65 nm MAPS





- Functional chips **ALPIDEs (180 nm)** have been bent routinely
- **Several ways** were explored (bending before/after bonding, different jigs)
- **The chips continue to work** (doi:10.1016/j.nima.2021.166280)
- Full mock-up called "**μITS3**": 6 ALPIDE chips, bent to ITS3 target radii
  - **Beam test** on μITS3: **uniform** among different radii

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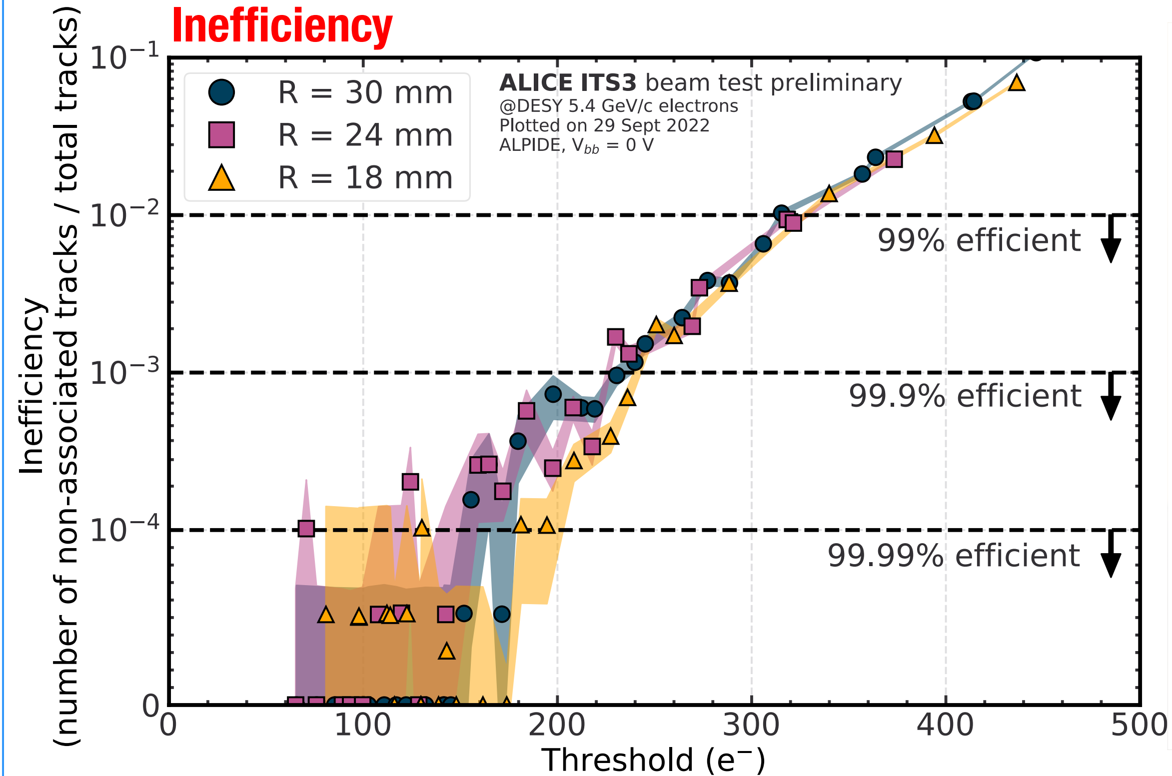
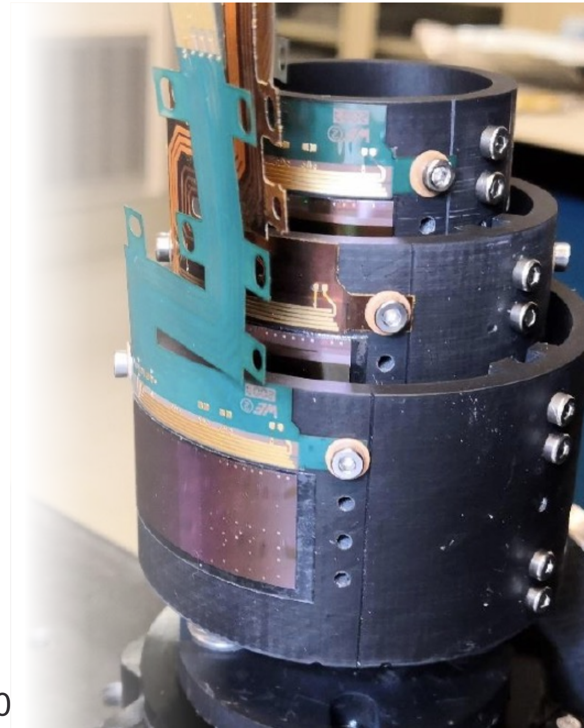
Bending of 180 and 65 nm MAPS





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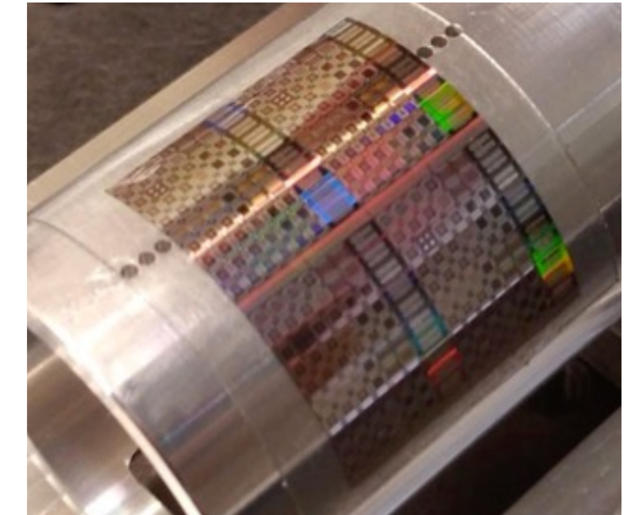
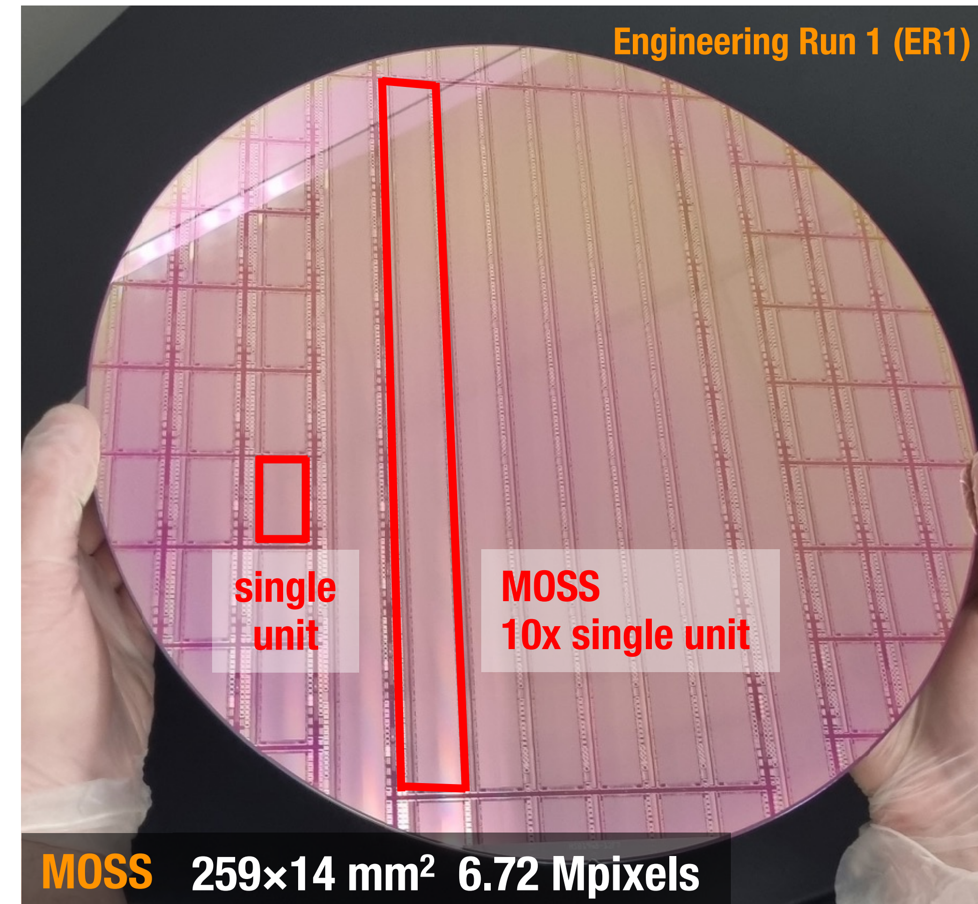
TPSCo 65nm chips bending of both APTS and DPTS



- special boards developed to bond on the bent structure
- tests ongoing
  - so far all test structures are working
  - more measurements and sample preparation ongoing

CMOS MAPS – Wafer scale sensors : stitching

- For large area (ALICE-ITS3 280 x 94 mm) → stitching needed:
  - aim at a realization of **a true single wafer scale sensor**
- Eliminates the need of tiling chips on circuit boards
- **First wafers just received** (ALICE-ITS3) → **MOSS** (asses the yield of wafer-scale stitched sensors, testability, not yet as sensor for ITS3)
  - **First CMOS MAPS for HEP using stitching**
  - to be thinned, diced…and tested



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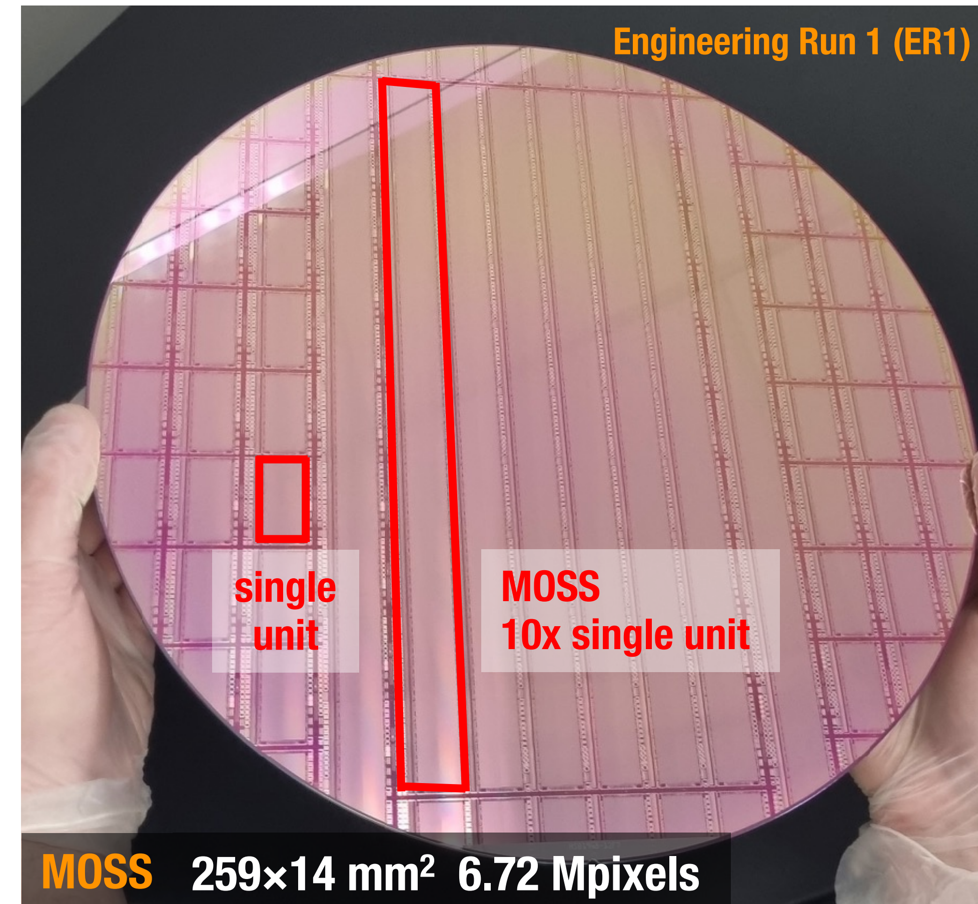
- **Very first single unit** (single-stitching) **tested** (two weeks ago!) in a probe station → **is alive!** can be powered and responds correctly to slow control commands

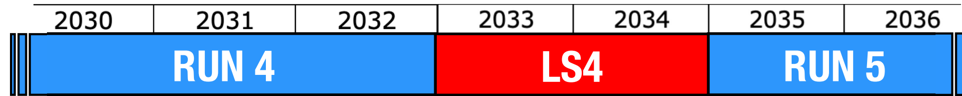


ALICE

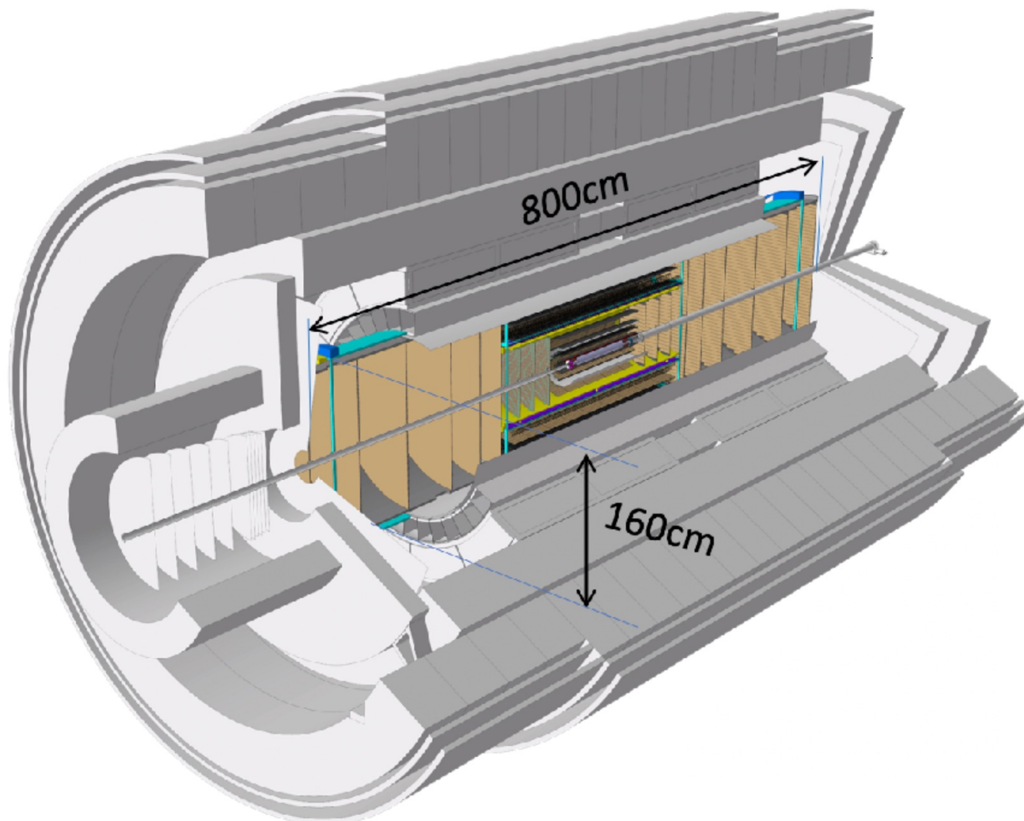
ALICE applications – ALICE 3

More about ALICE3 performances and physics motivations in **"ALICE upgrades"**, **R. H. Munzer, 25/05 17:24**

LHC **LS4**, 2033/34



ALICE 3 : a next-generation LHC heavy-ion (soft QCD) experiment



Outer tracker with around **60 m² MAPS** tracker

- order of magnitude **larger** than ITS2
- large coverage: ±4η
- high-spatial resolution: ≈ 5 µm
- very low material budget: X/X_0 (total) ≲ 10%
- low power consumption ≈ 20 mW/cm²

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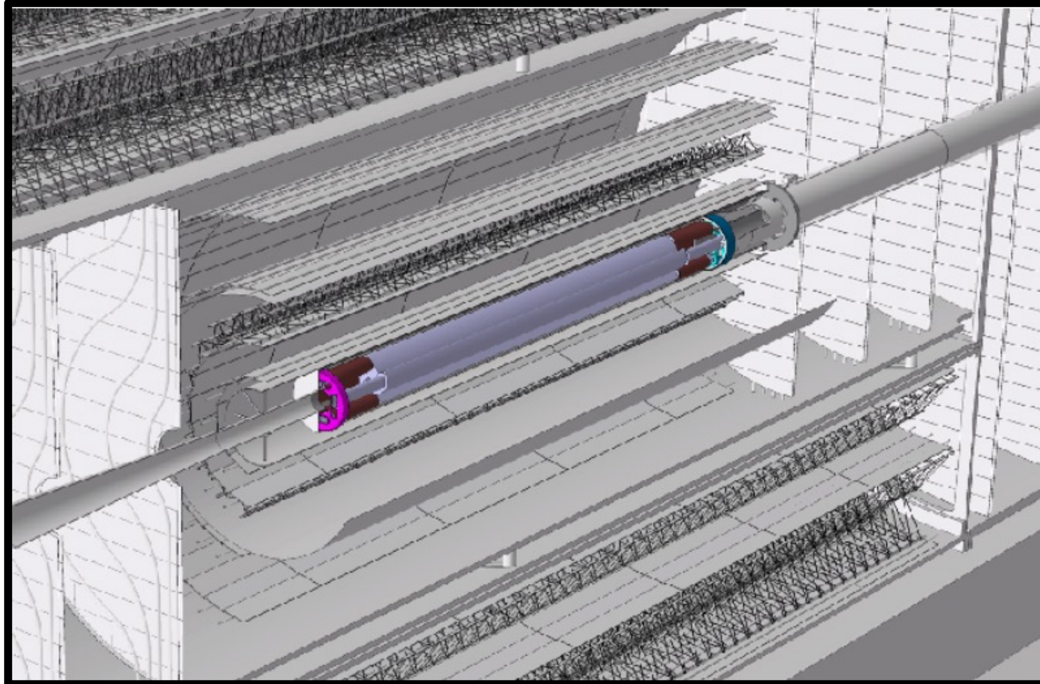
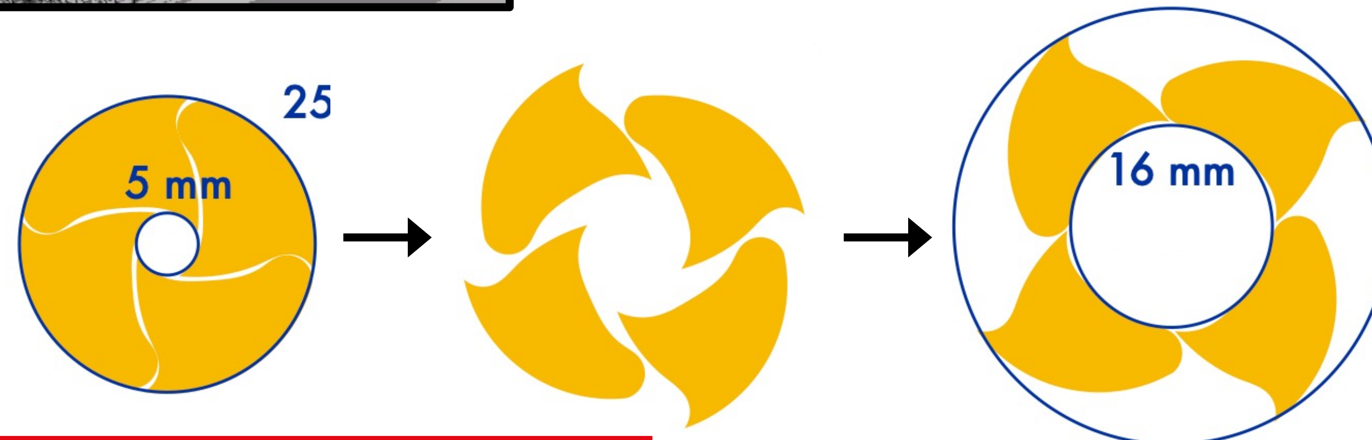


Innermost layers (**vertex detector**)

- will be based on wafer-scale, ultra-thin, curved MAPS "**iris tracker**" → **ITS3 like BUT in vacuum**
  → 3 layers **inside beampipe, retractable configuration**
- clear **extension of ITS3 developments**
- pushes the **technology** on a number of fronts
  - distance from interaction point: 5 mm
  - radiation hardness ~ 10^{16} 1MeV n_{eq}/cm^2
  - spatial resolution: ≈ 2.5 µm
  - material budget: ≈ 0.1%X_0/layer



→ The next big and concrete step for CMOS MAPS

Conclusions

CMOS MAPS are ideal devices for vertexing
Low material budget (thin + low power), high resolution (small pixels), large surfaces (commercial process), non-planar geometries (thin silicon is flexible)

Impressive progress over the last decade
Already several applications, e.g. STAR 2015 and ALICE ITS2 2021, and improvements on radiation hardness, low noise, and speed

ALICE ongoing R&D on bending, deeper sub micron tech. node (65 nm) and stitching (wafer scale)
Big push from ITS3 (2026): new inner-most 3 layers, wafer-scale, bent, stitched sensors → paves the way for future experiments like ALICE 3 (2033): 60 m^2 silicon-only

Lot of interest on ALICE ITS3 developments from other experiments
Similarly to what happened with ITS2