FASER Experiment: Ongoing and Proposed Upgrades

Stefano Zambito, on behalf of the FASER collaboration

Large Hadron Collider Physics Conference 2023

Belgrade, 25-5-2023

Introduction & Outline

Today's talk:

- FASER detector rationale
- Upgrade of preshower
  - ↳ monolithic silicon pixel ASIC
- Upgrade of calorimeter readout scheme
- FASER(ν)2 at Forward Physics Facility (FPF)

Check these out too!

- Noshin: *first dark photon search results*
- Tobias: *neutrinos in the forward region*
- Rosham: *new physics searches at FPF*

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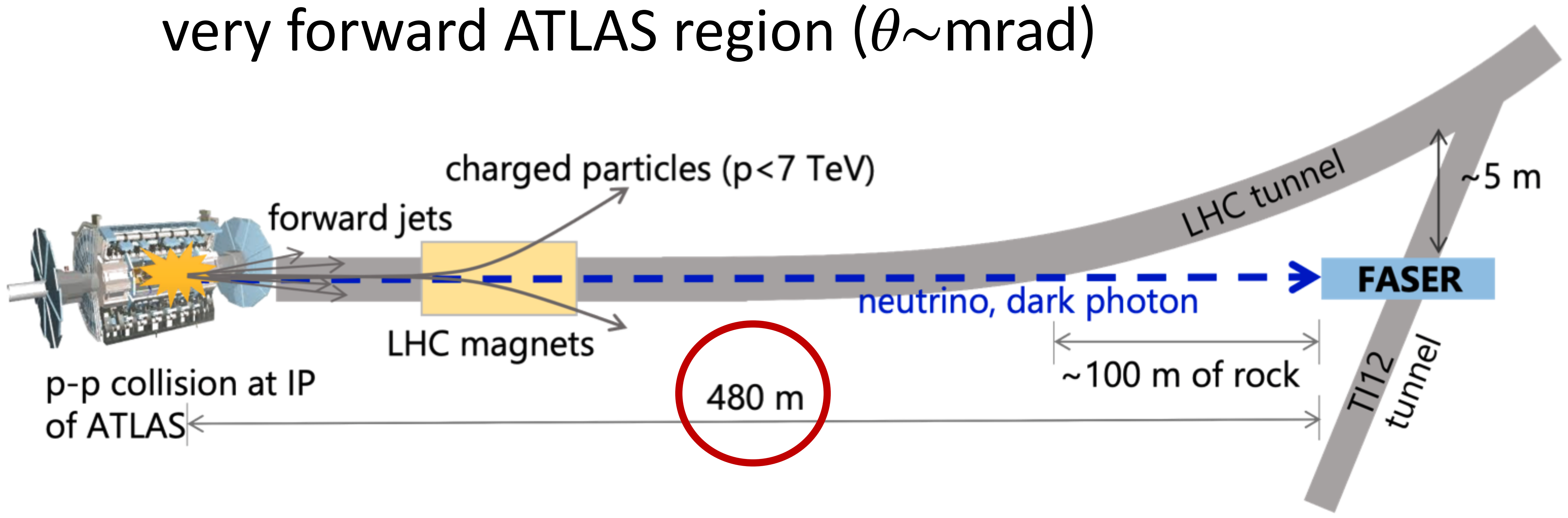
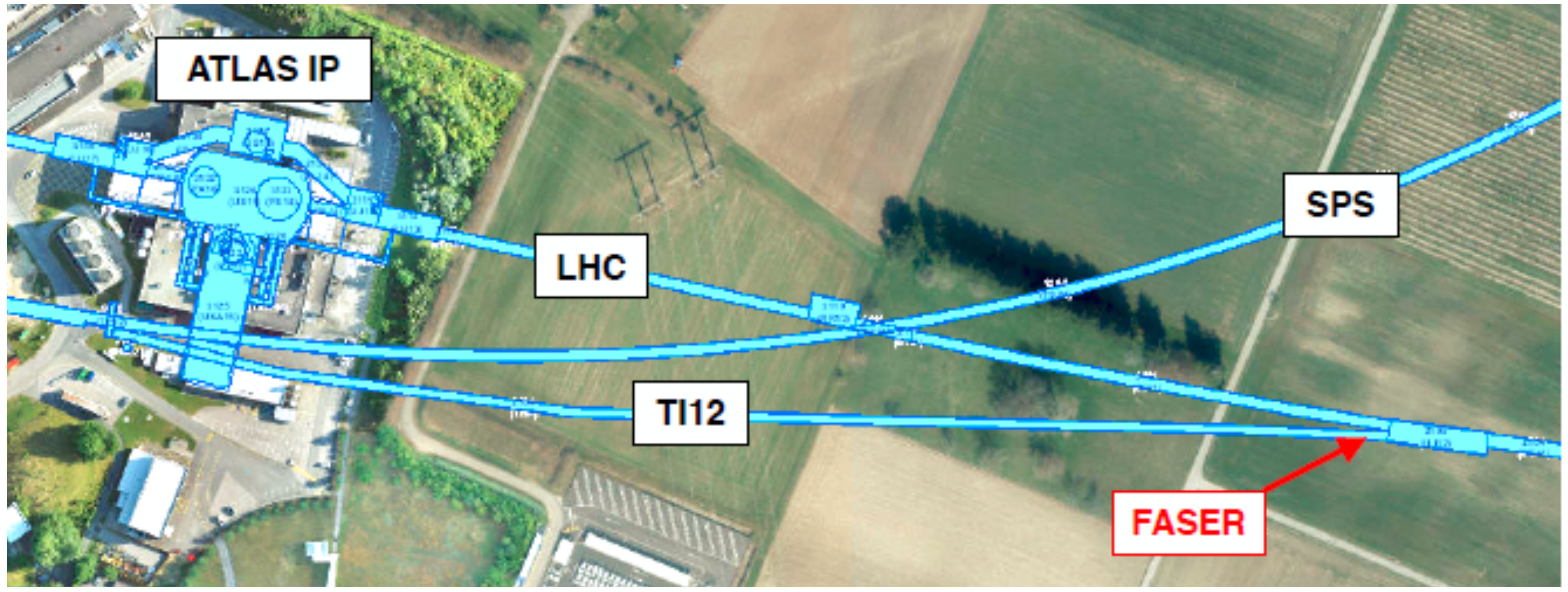
The ForwArd Search ExpeRiment at the LHC

Search for light, weakly interacting (LLP) new particles

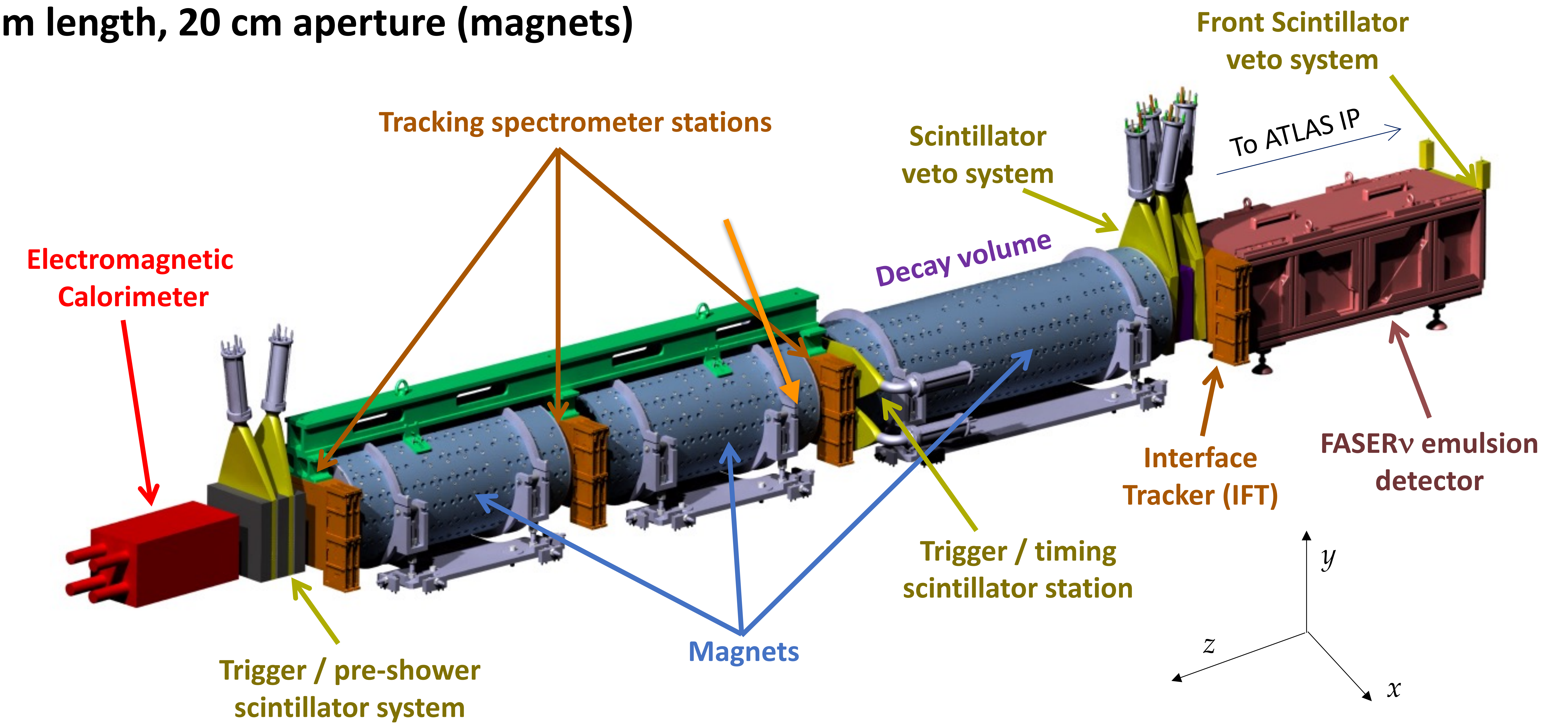
↳ stemming from rare meson decays (π, η, K, D ...) in very forward ATLAS region ($\theta\sim$mrad)





The FASER Experiment

≃7 m length, 20 cm aperture (magnets)



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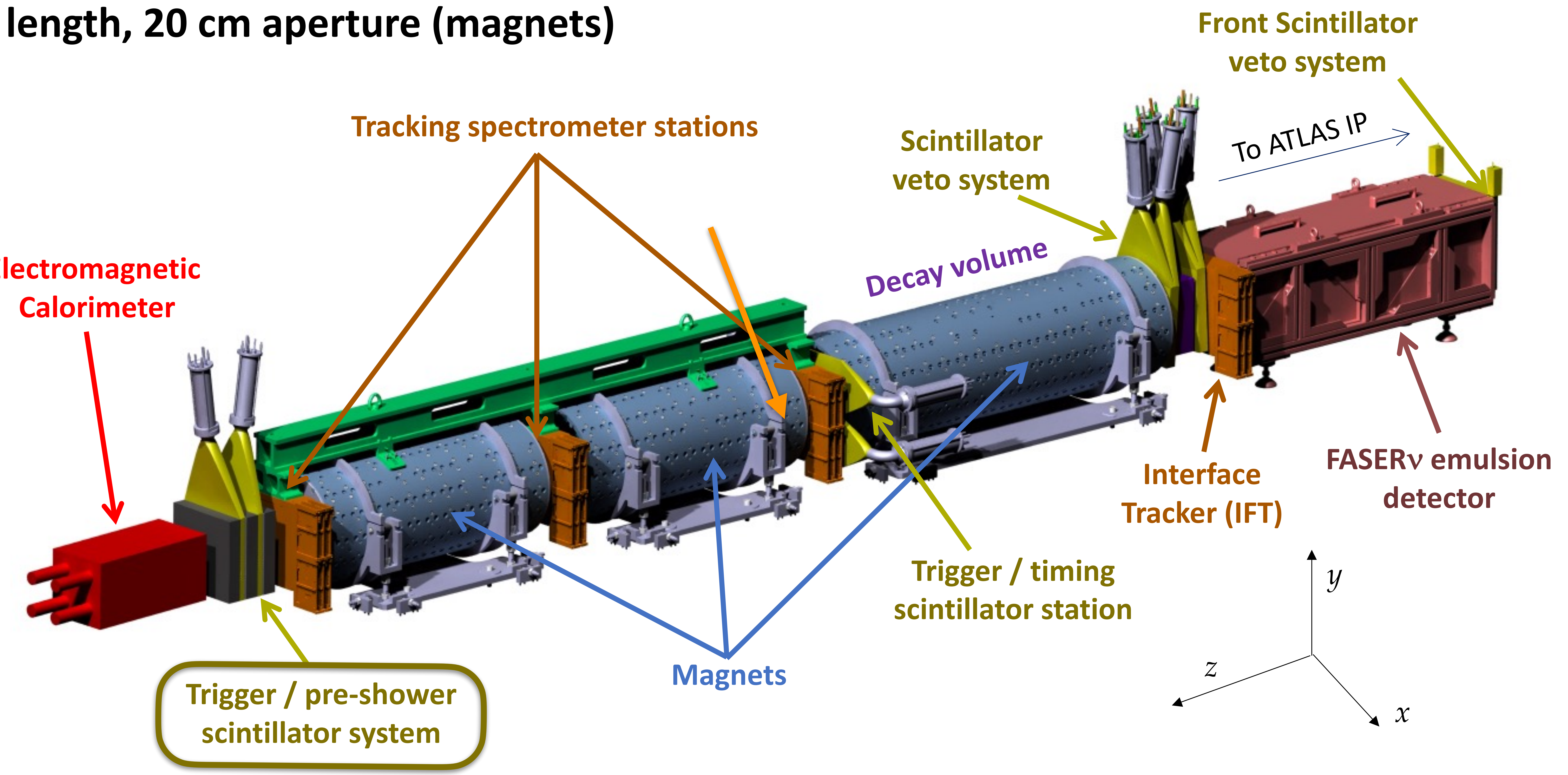
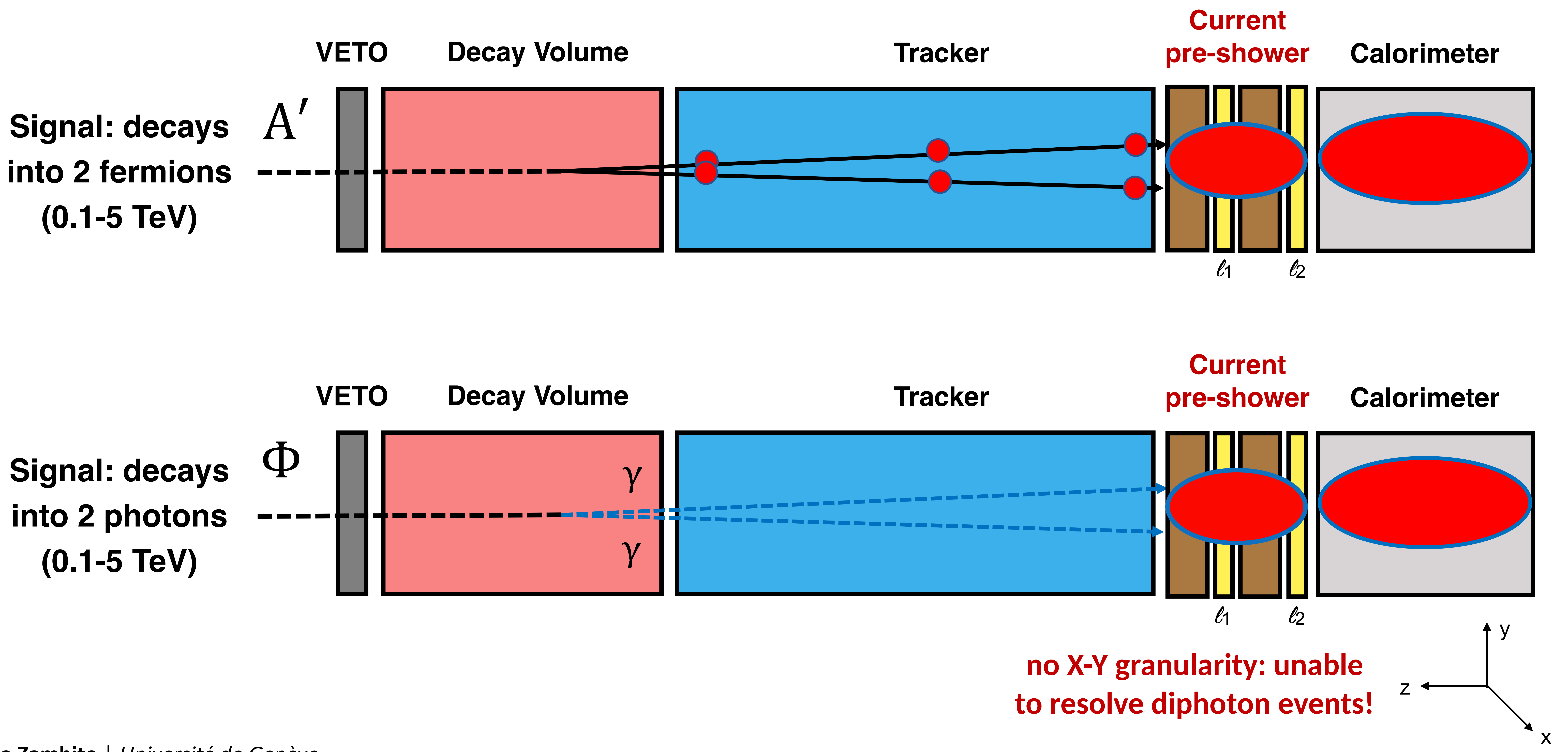
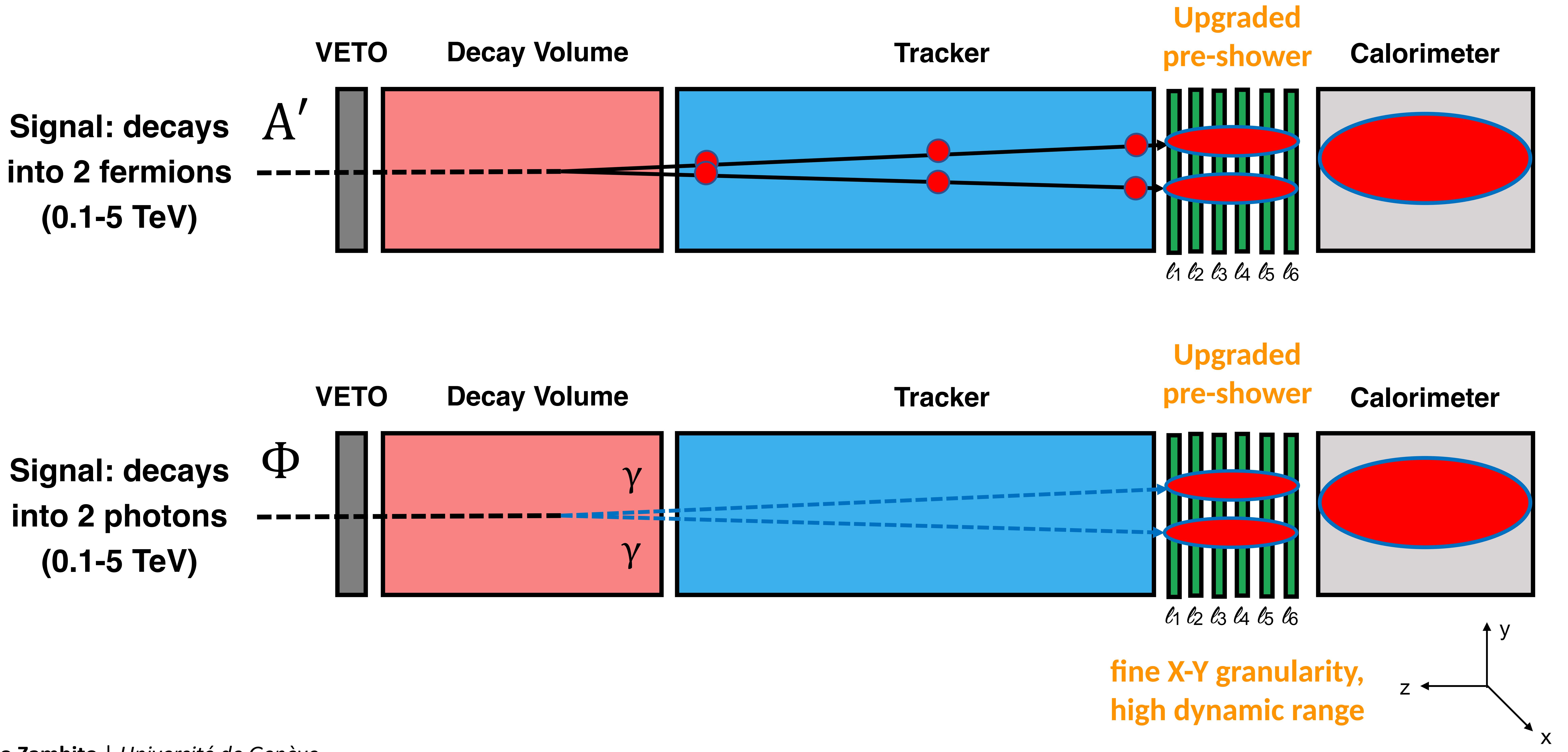


2 tungsten layers (2 X_0) + 2 graphite layers + 2 scintillators

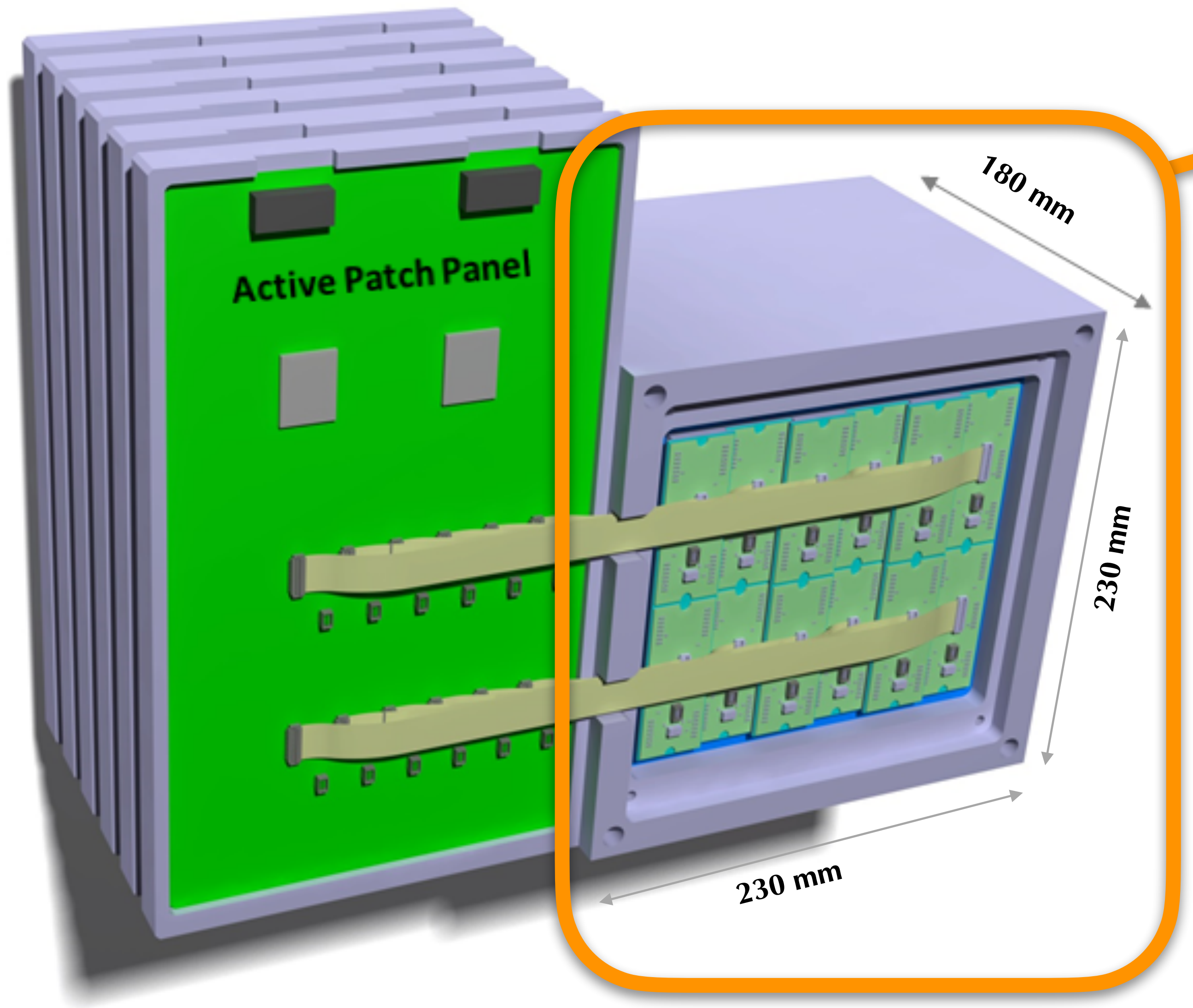
Current Detection Capabilities: Two Fermions



Desired Detection Capabilities: Two Fermions / Photons

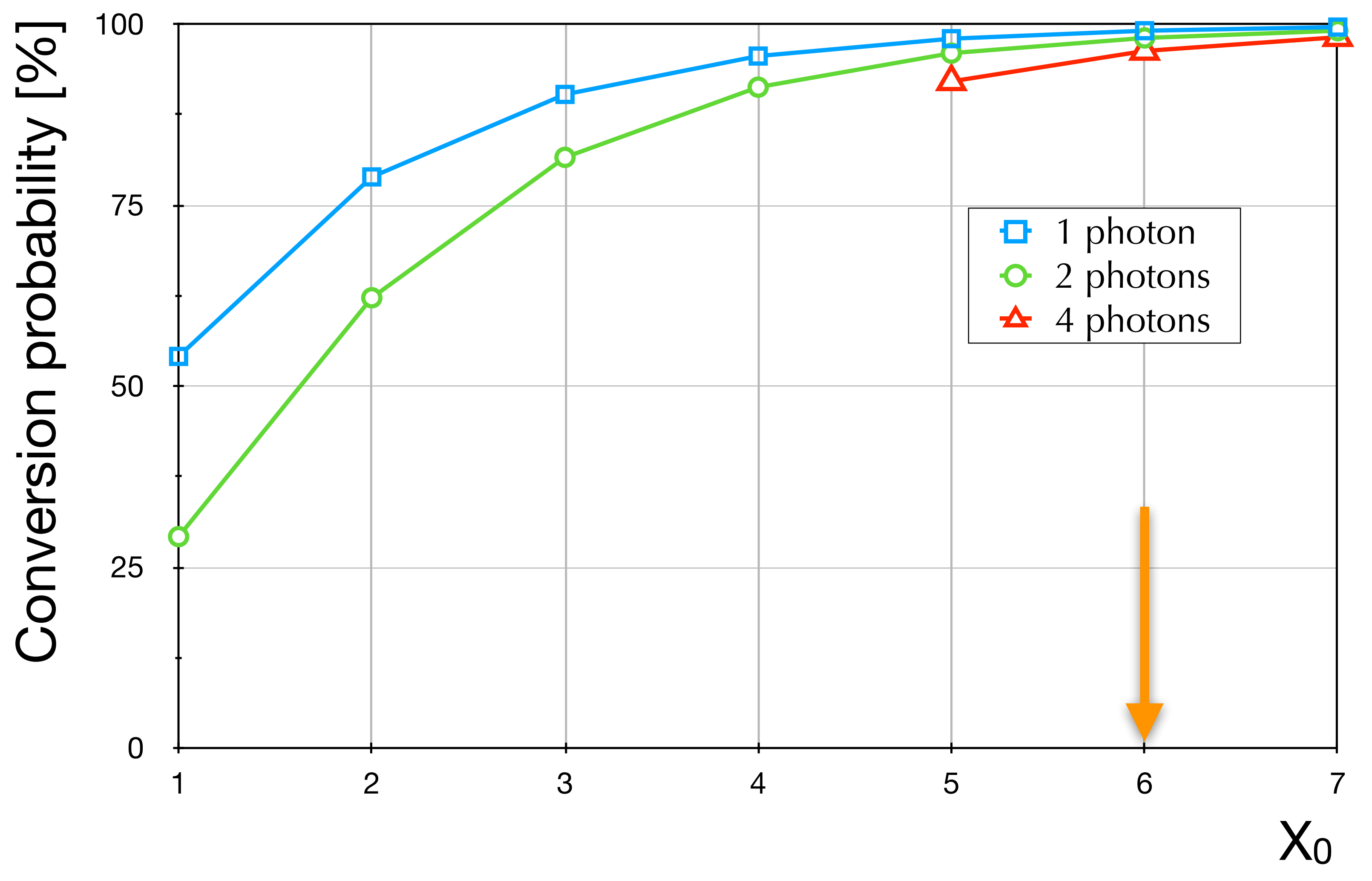


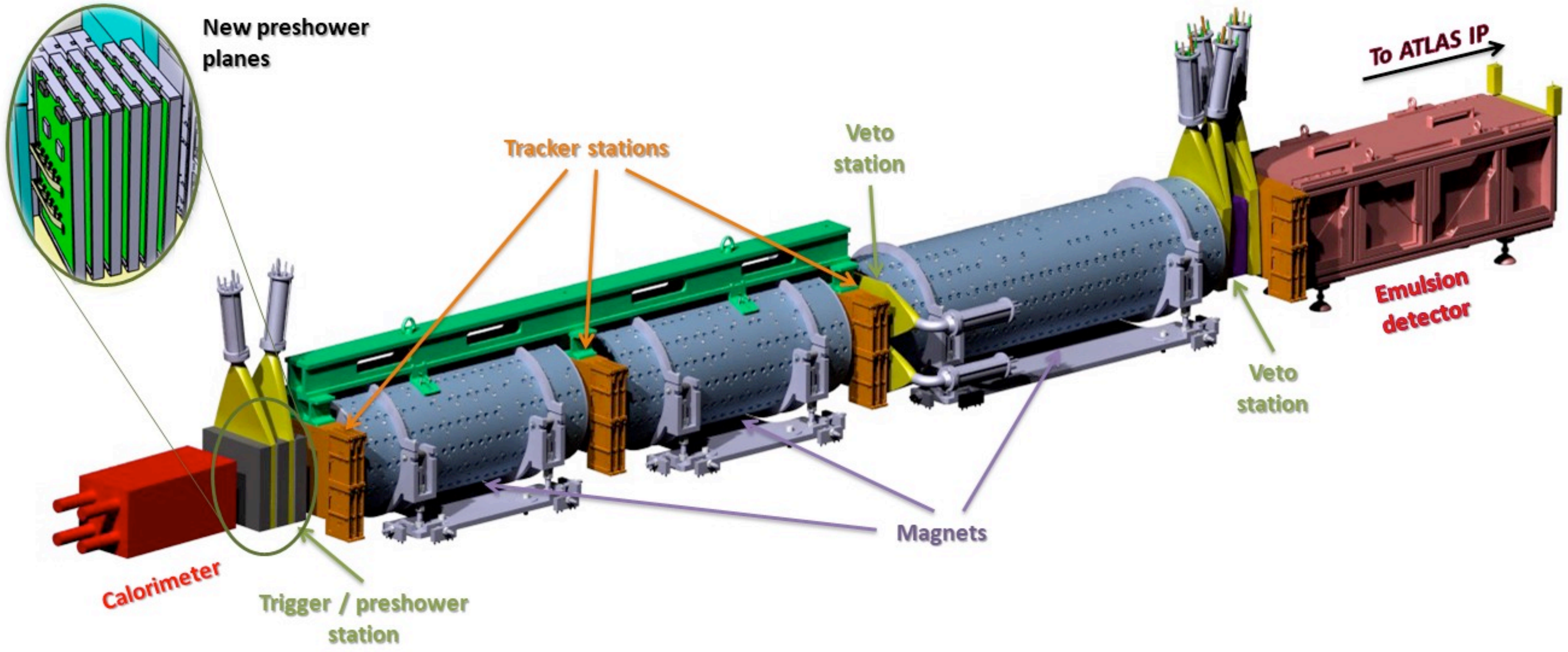
New Preshower Detector [I]



Upgraded preshower detector

- 6 detector planes + 2 scintillators
  - ↳ each plane: 1 X_0 tungsten + monolithic Si pixel sensors
- project approved by CERN: CERN-LHCC-2022-006
- targeting installation in 2024, during LHC Run 3

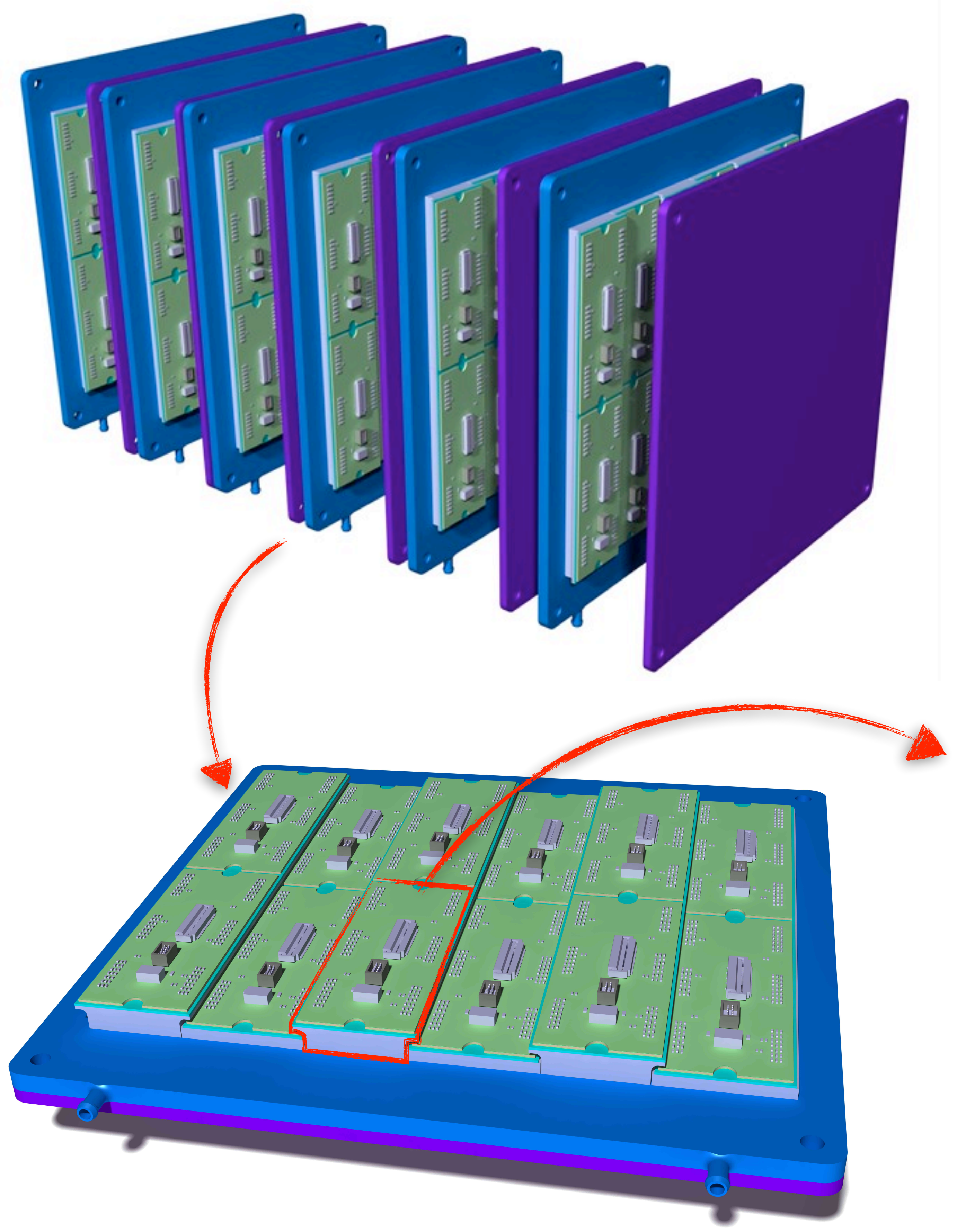




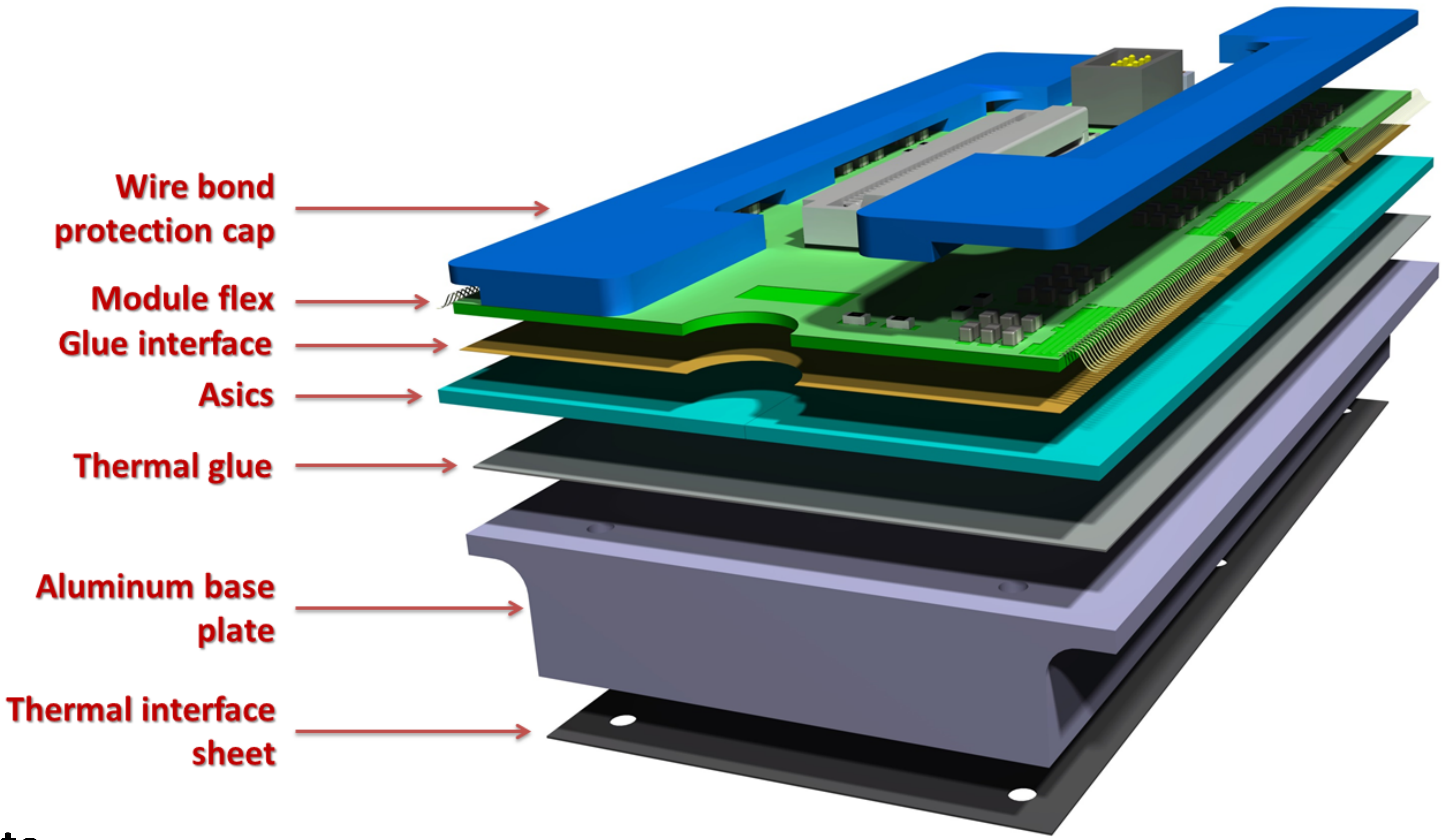
New Preshower Detector [II]

6 planes in total (silicon detector + W plate)

6 ASICs per module, 208x128 pixels each



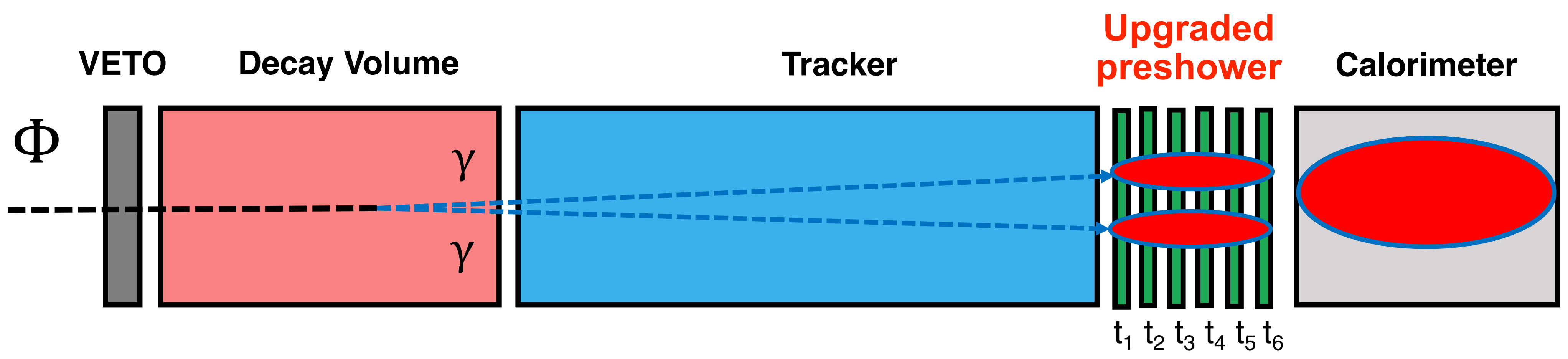
12 modules per plane, on cooling plate

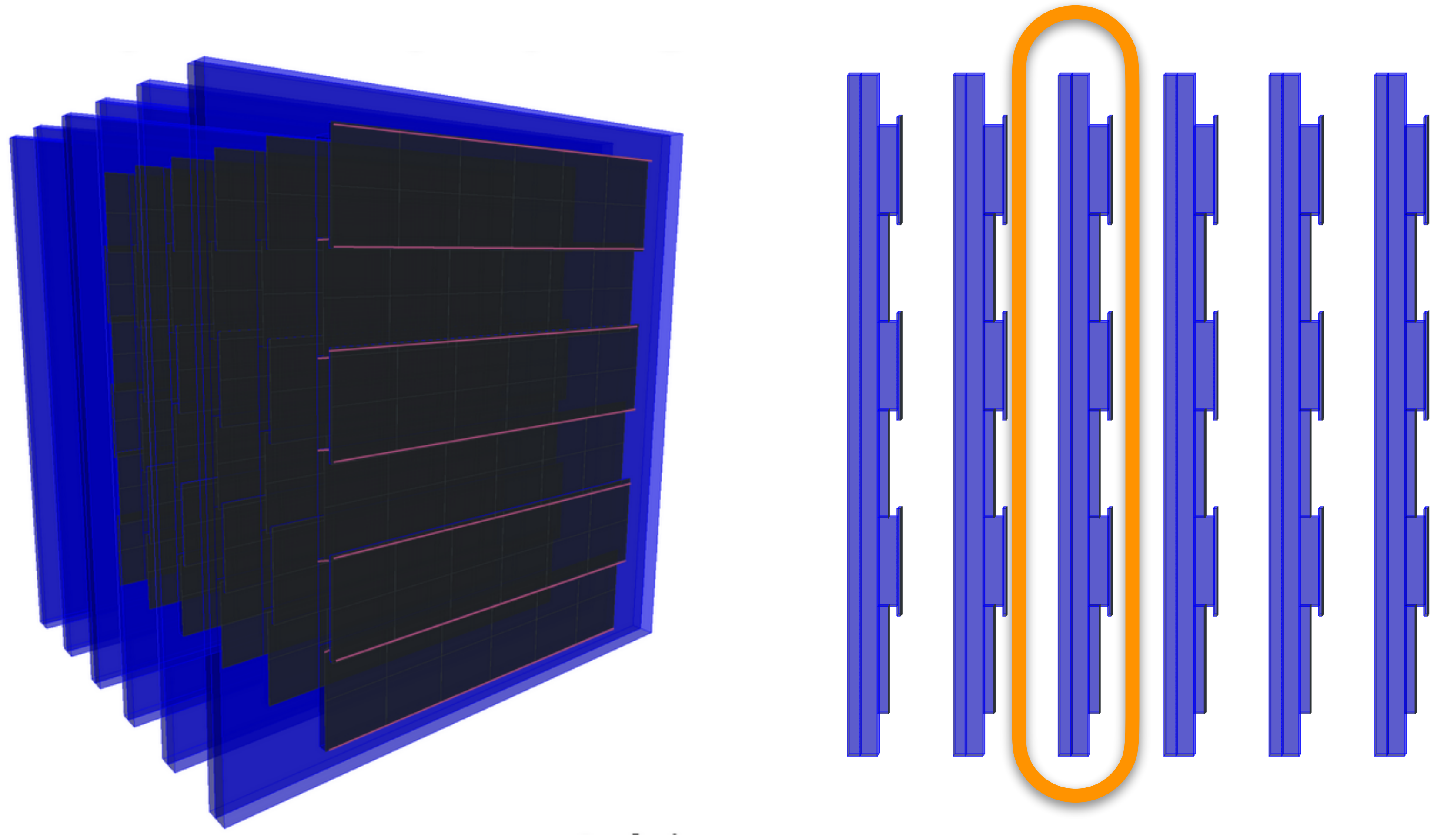


Preshower Simulation: Diphoton Signature

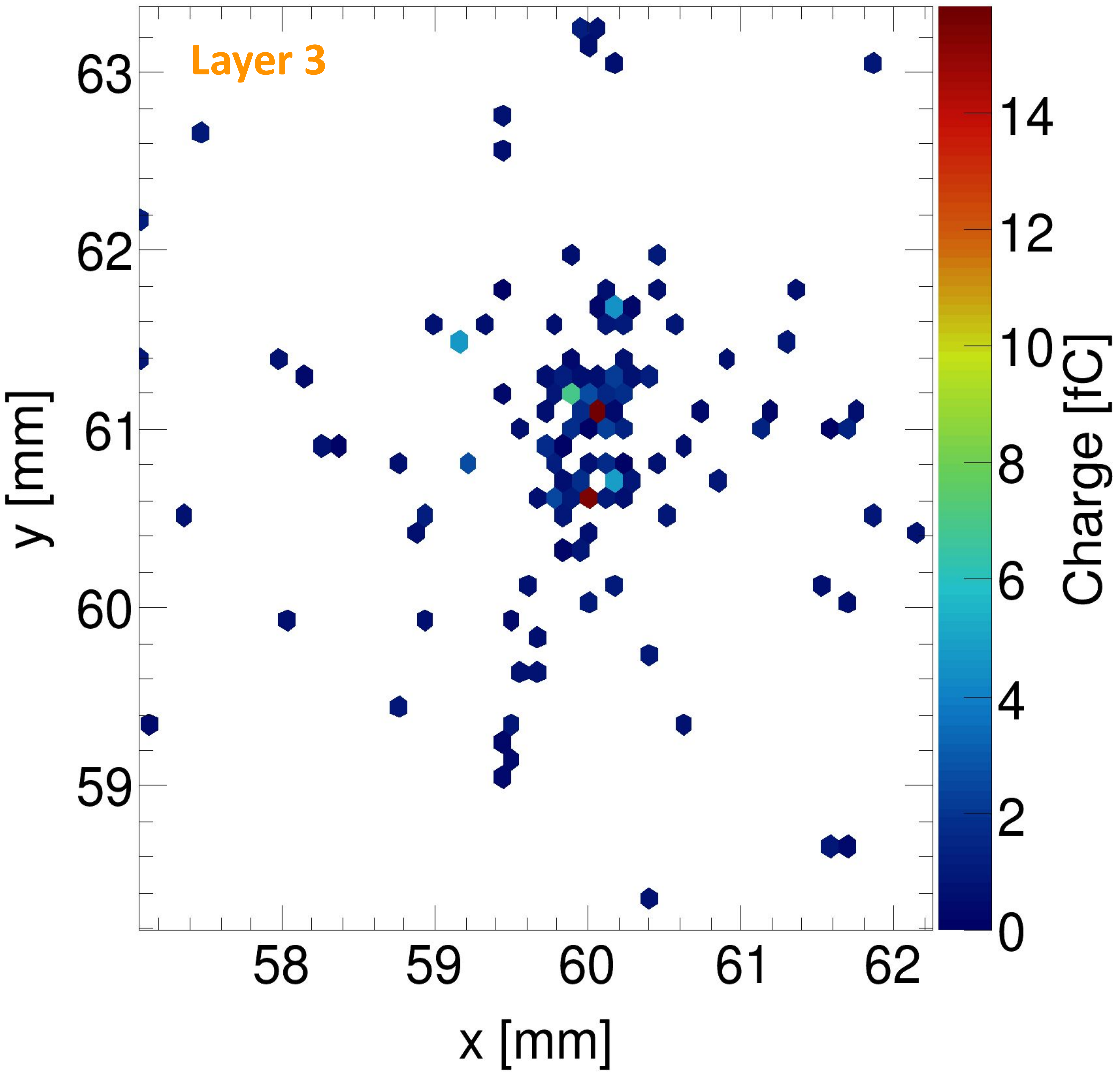
Simulating two photons:

$E\gamma$=1 TeV, $\Delta R\gamma$=0.5 mm





Layer 3



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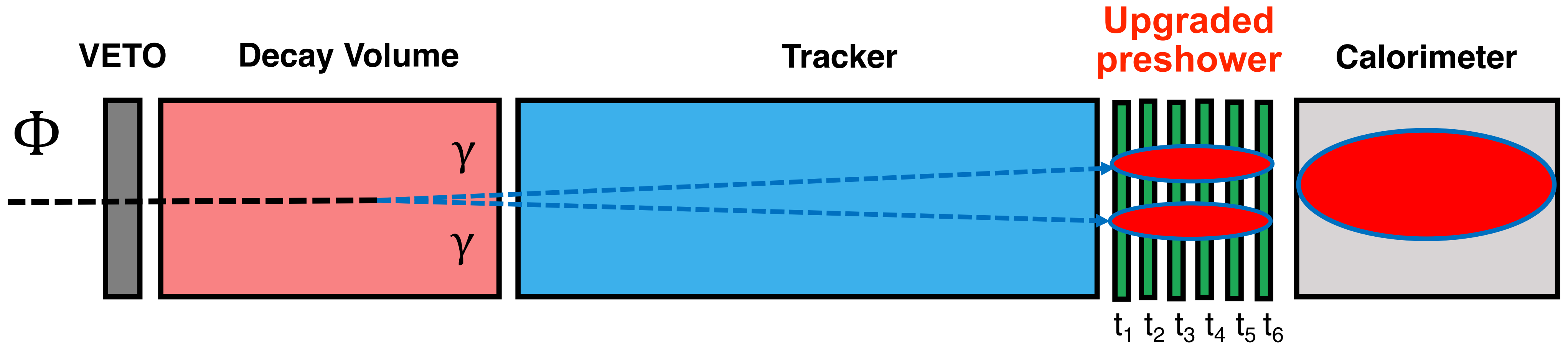

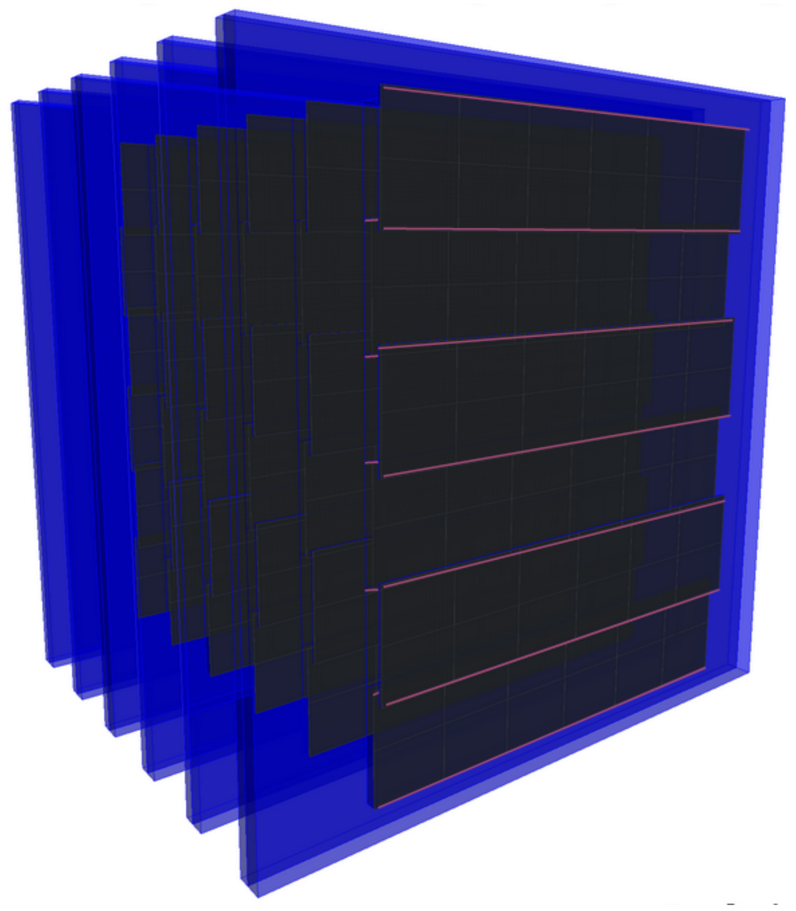

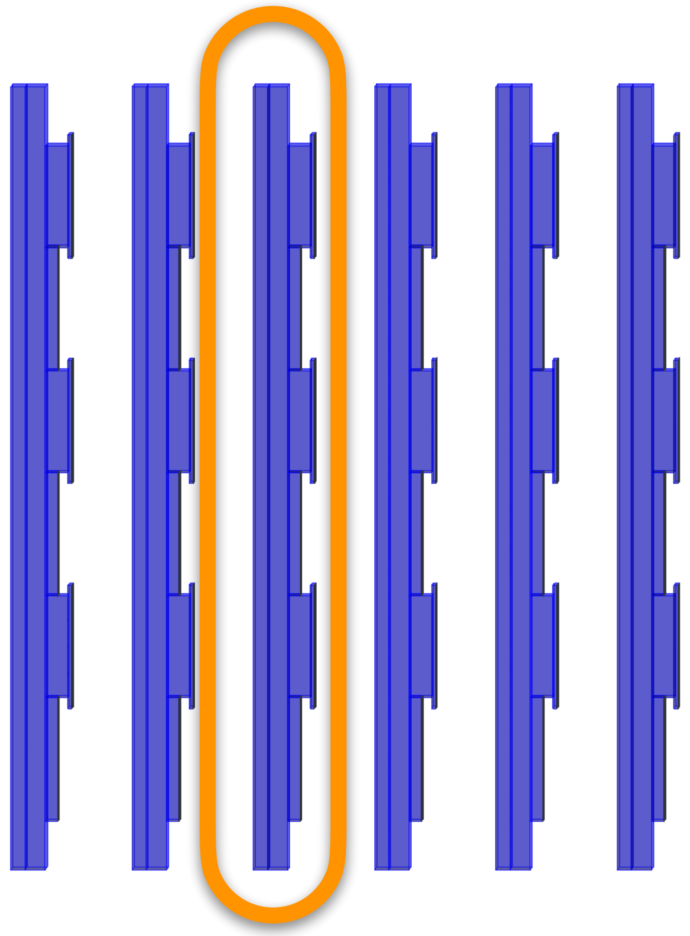

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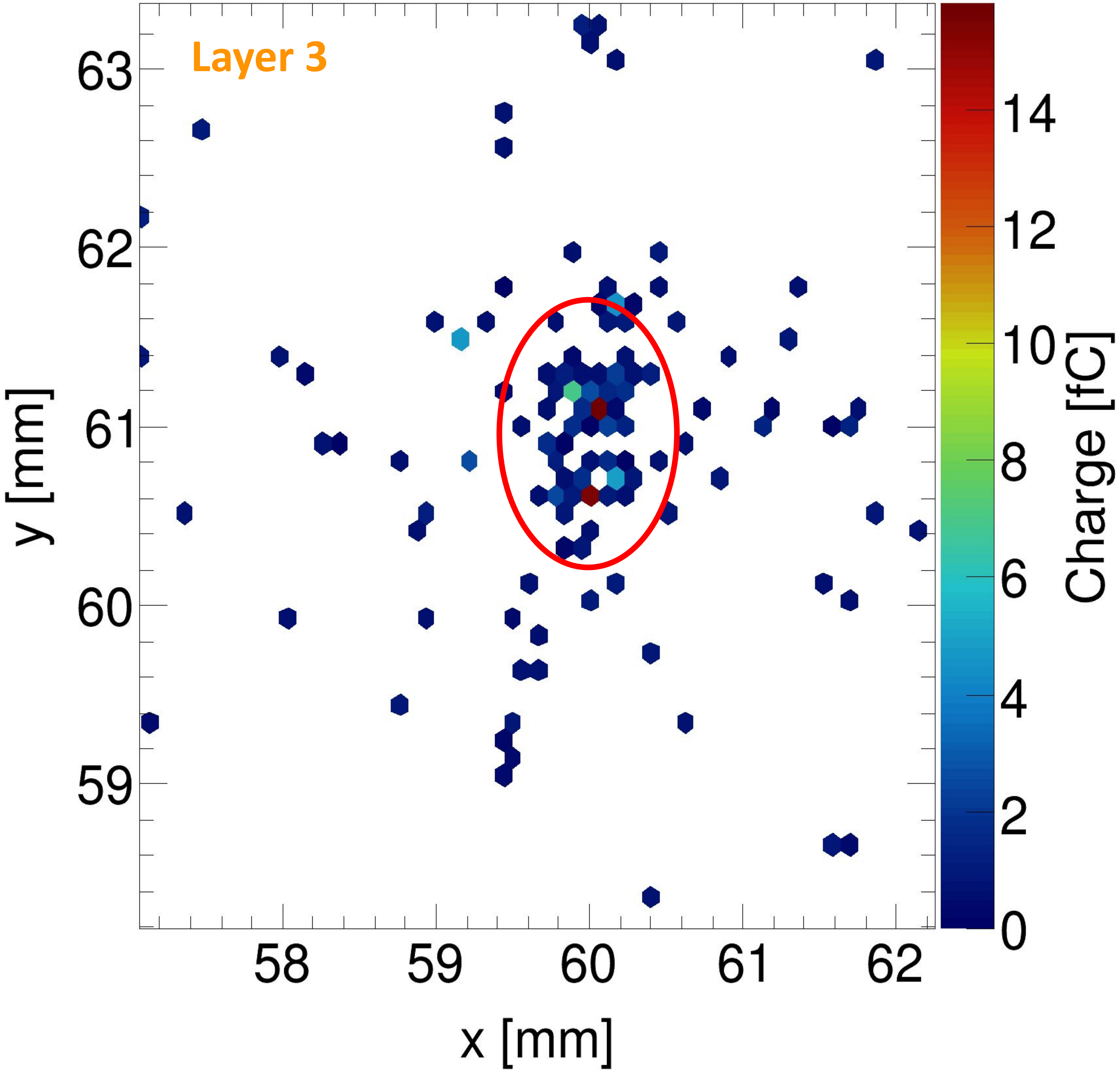

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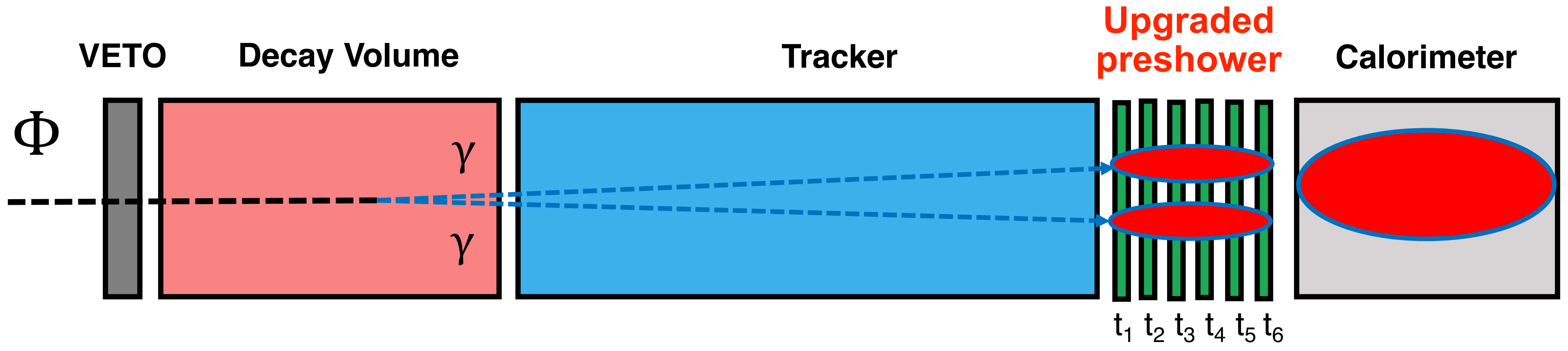

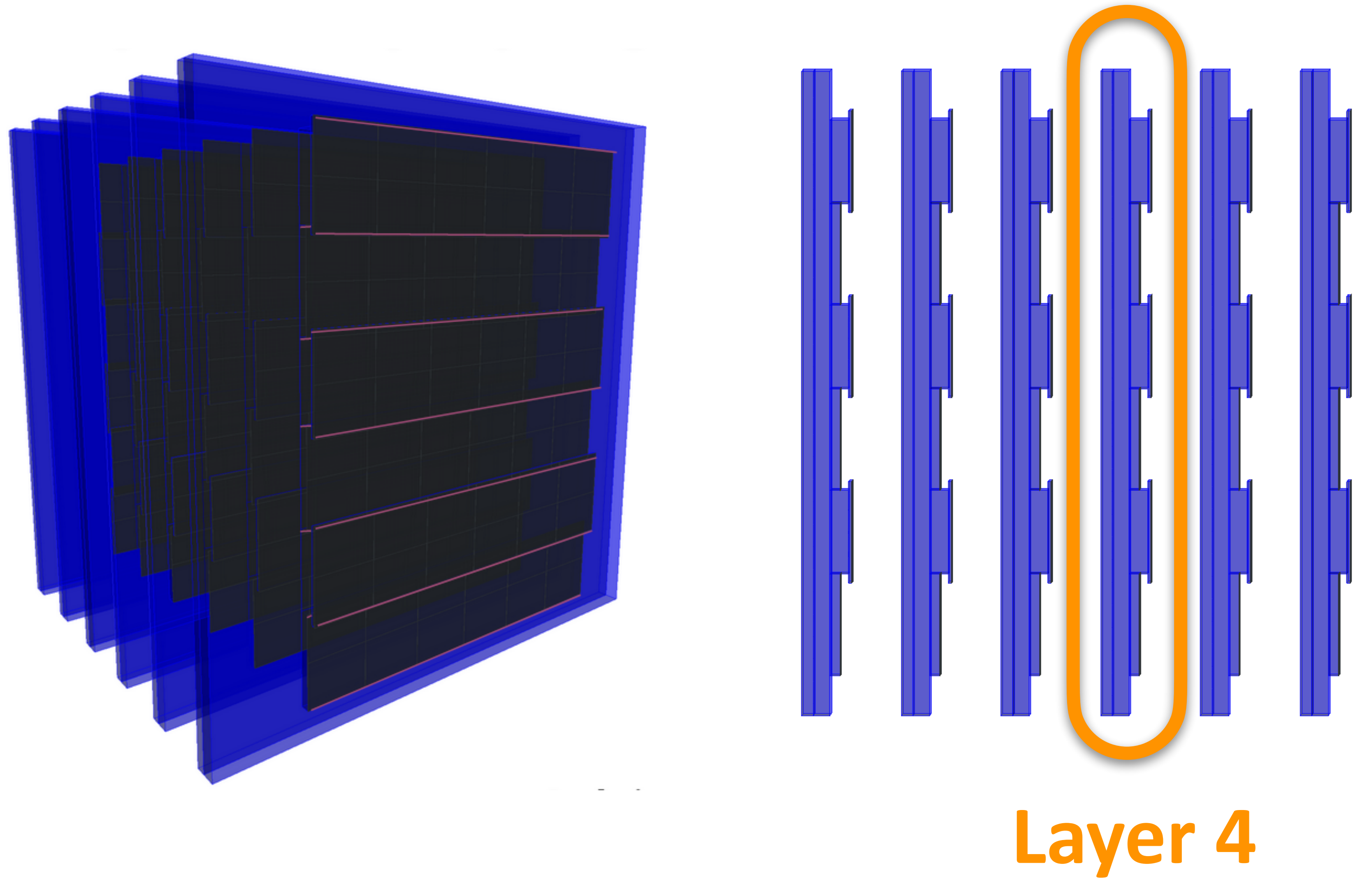

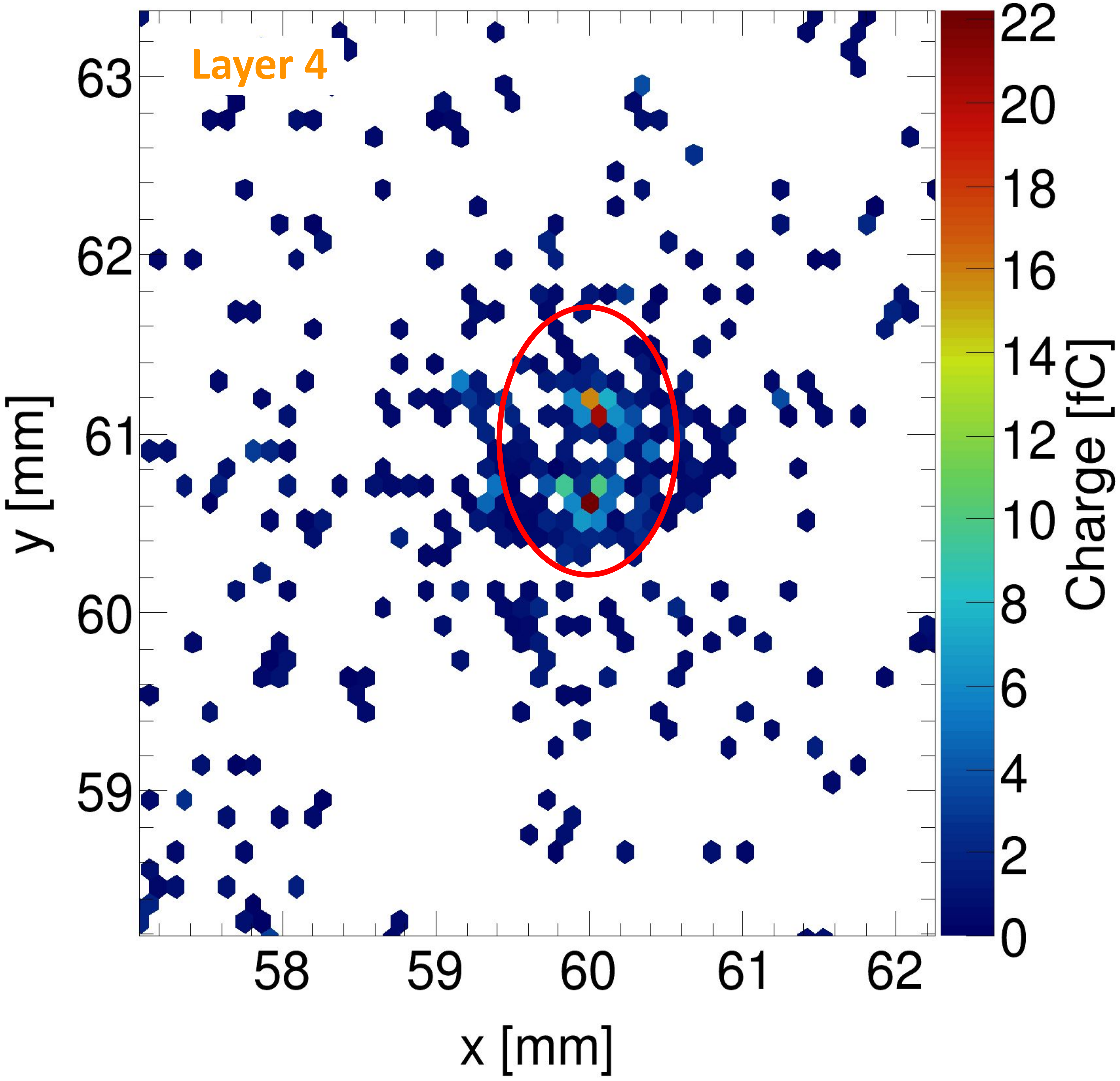

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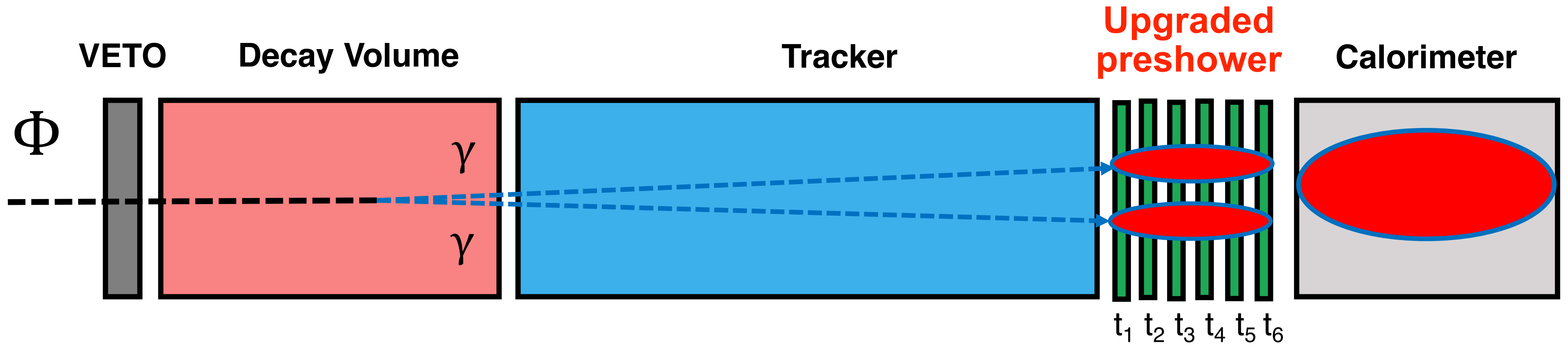

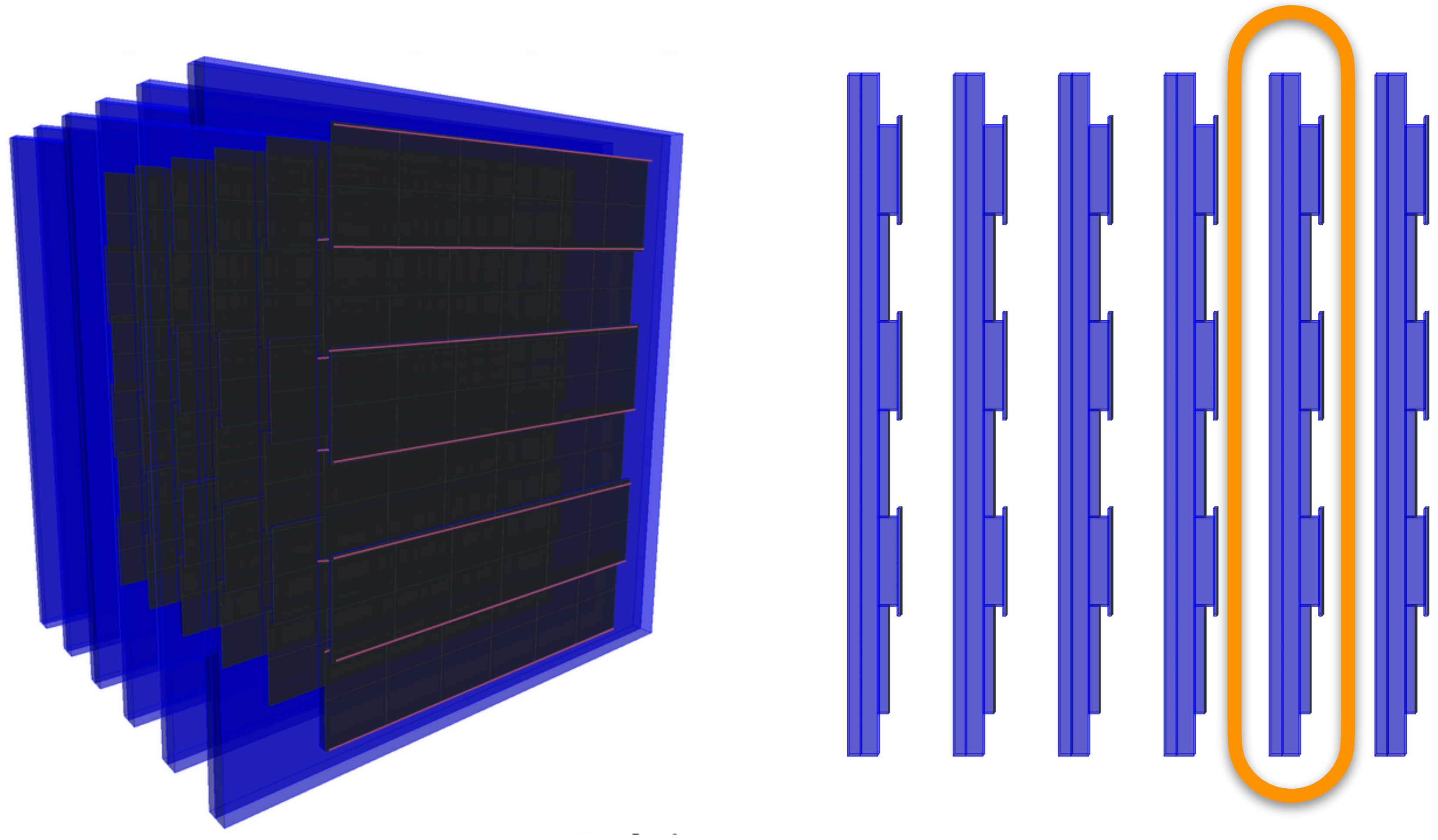

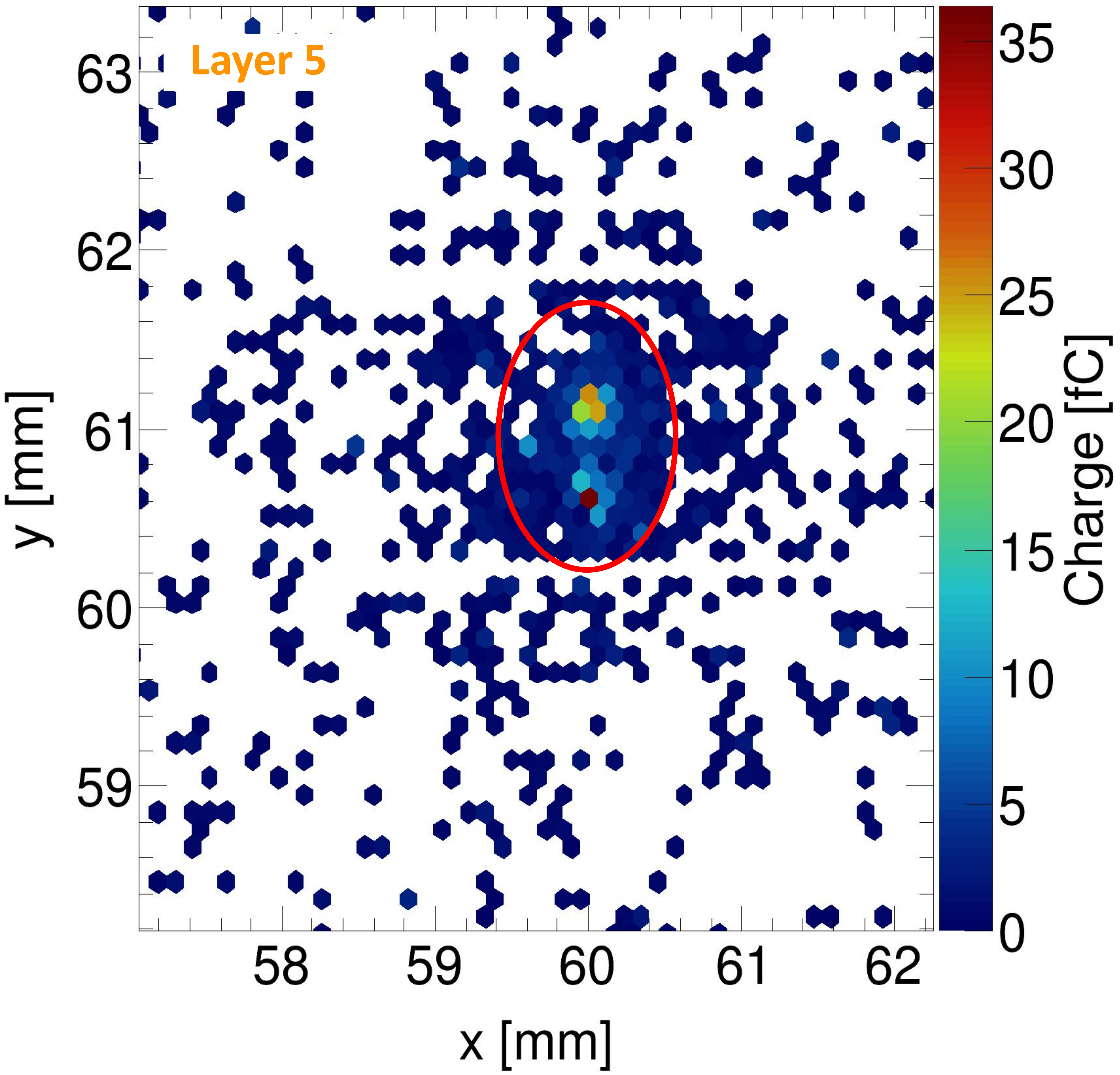

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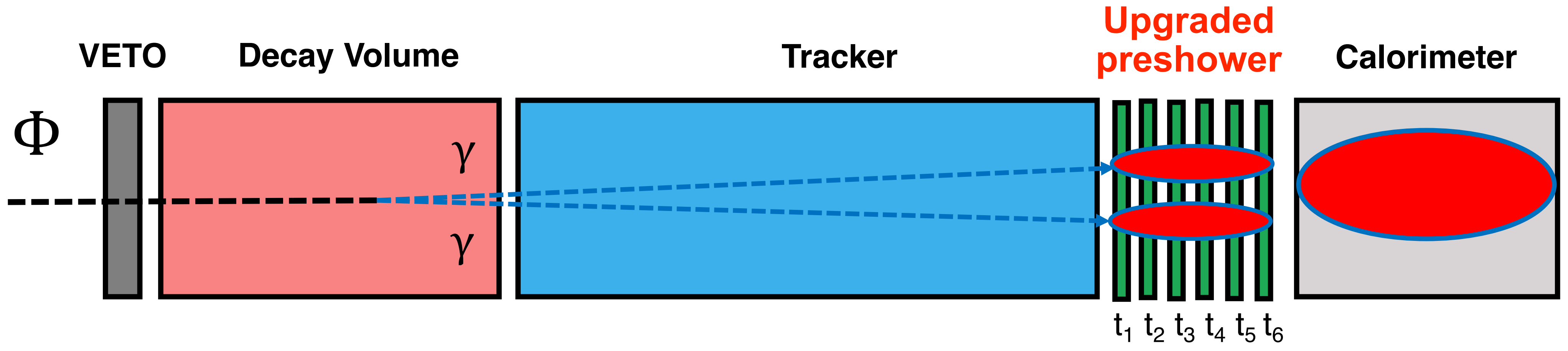
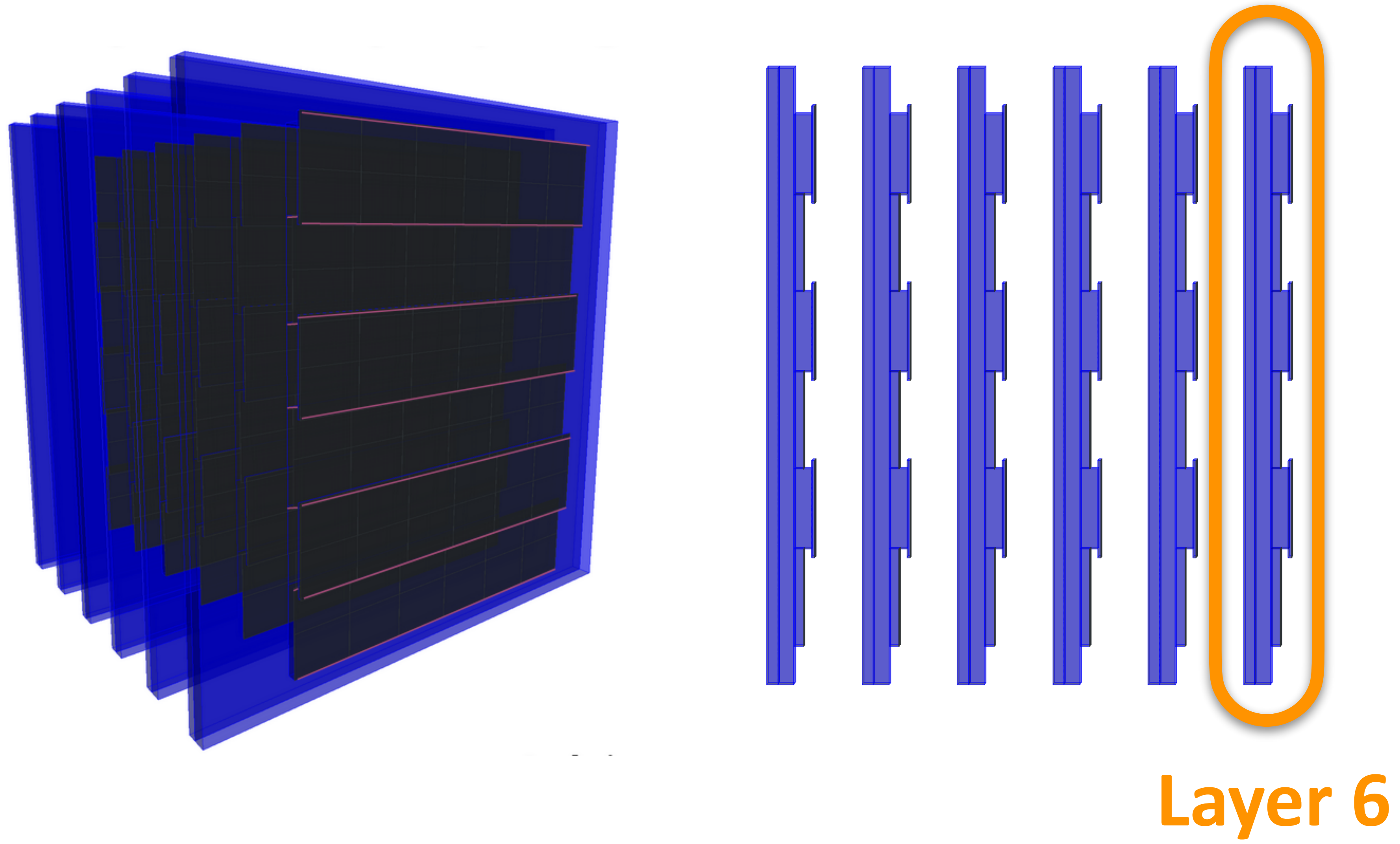
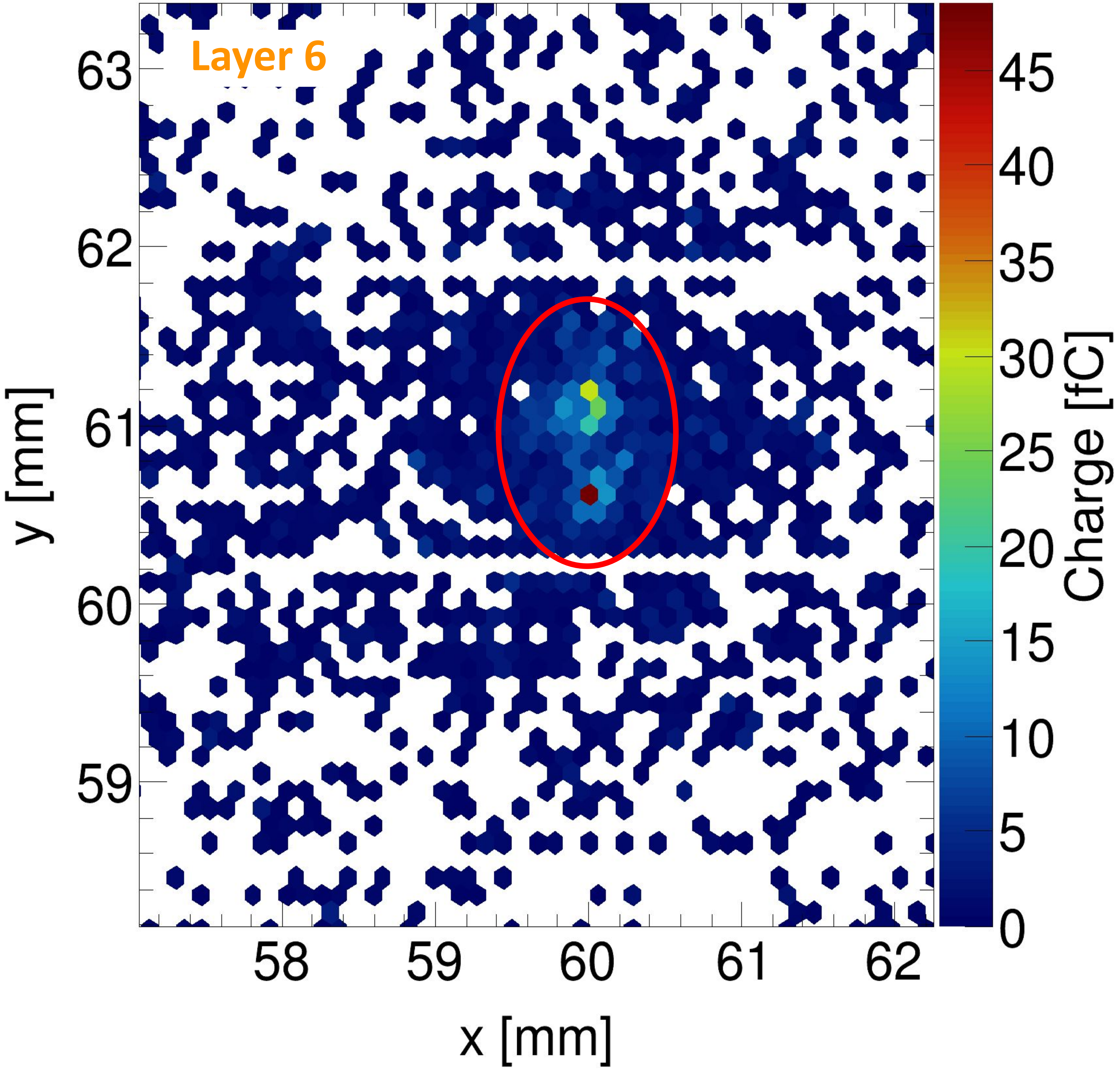
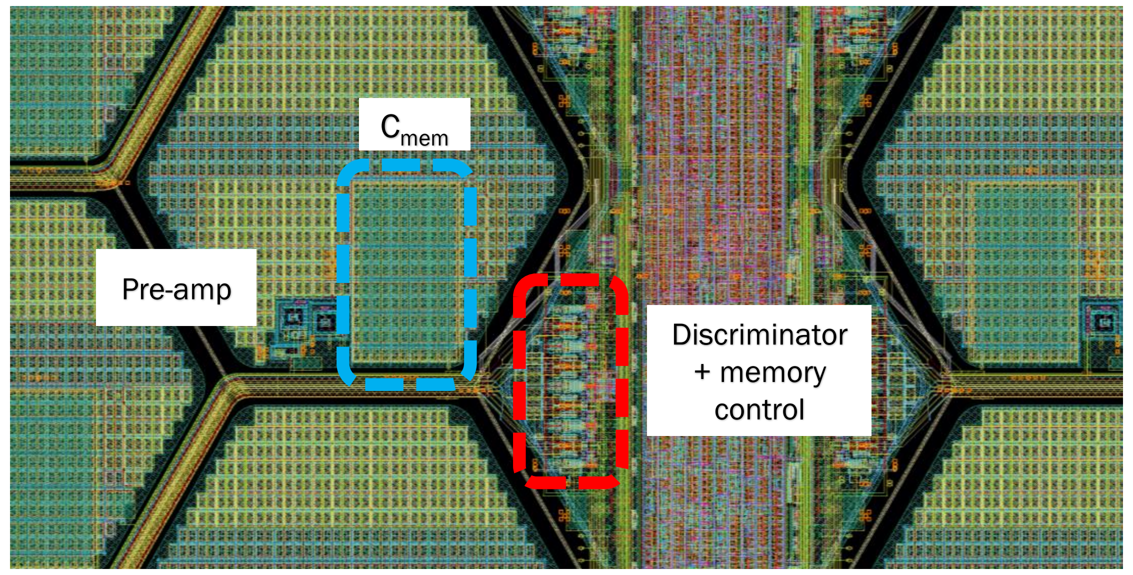




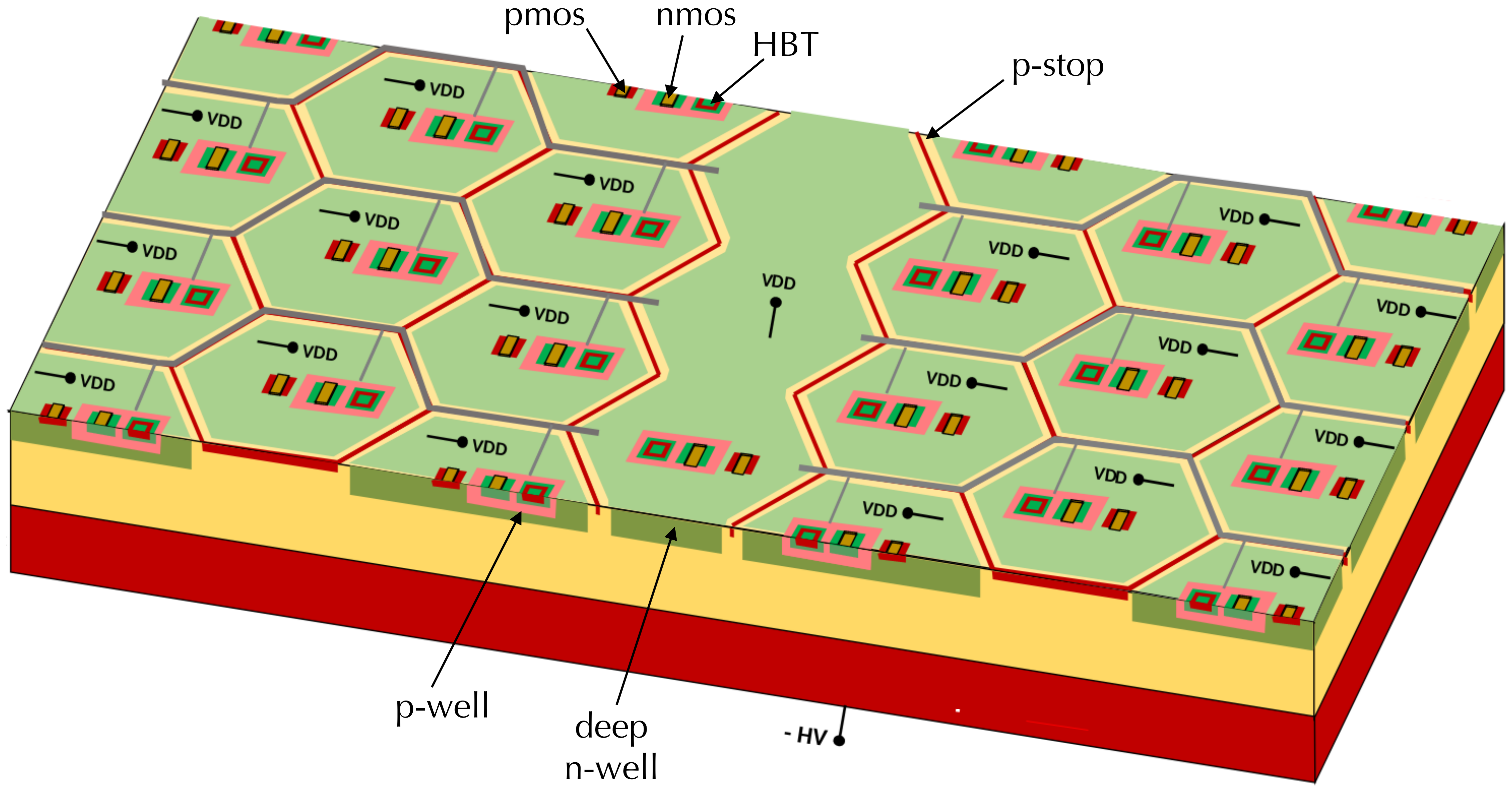


Monolithic Pixel ASIC: Sensor

Monolithic active pixel sensor
130 nm SiGe BiCMOS technology (IHP SG13G2)

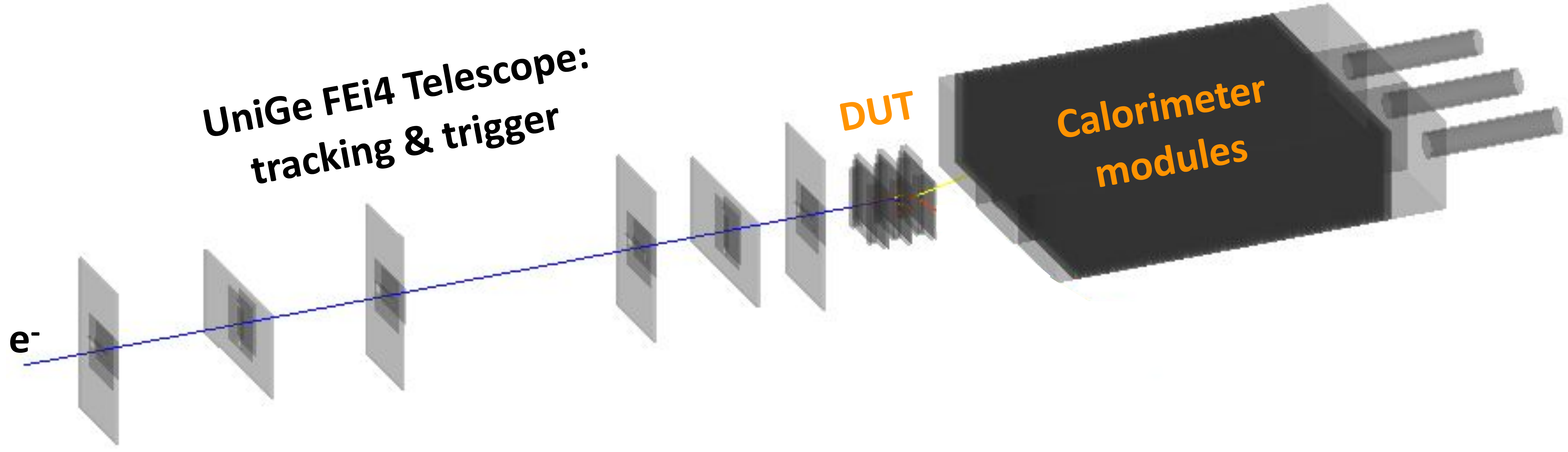


- High-resistivity (220 Ω·cm) substrate, about 130 µm thickness
- Hexagonal pixels integrated as triple wells; 80 fF pixel capacitance
- High dynamic range for charge measurement (0.5÷65 fC); fast readout of many channels



Main specifications	
Pixel Size	65 µm side (hexagonal)
Pixel dynamic range	0.5 ÷ 65 fC
Cluster size	O(1000) pixels
Readout time	< 200 µs
Power consuption	< 150 mW/cm^2
Time resolution	< 300 ps

September 2022: CERN SPS Test Beam (20-150 GeV e^-)



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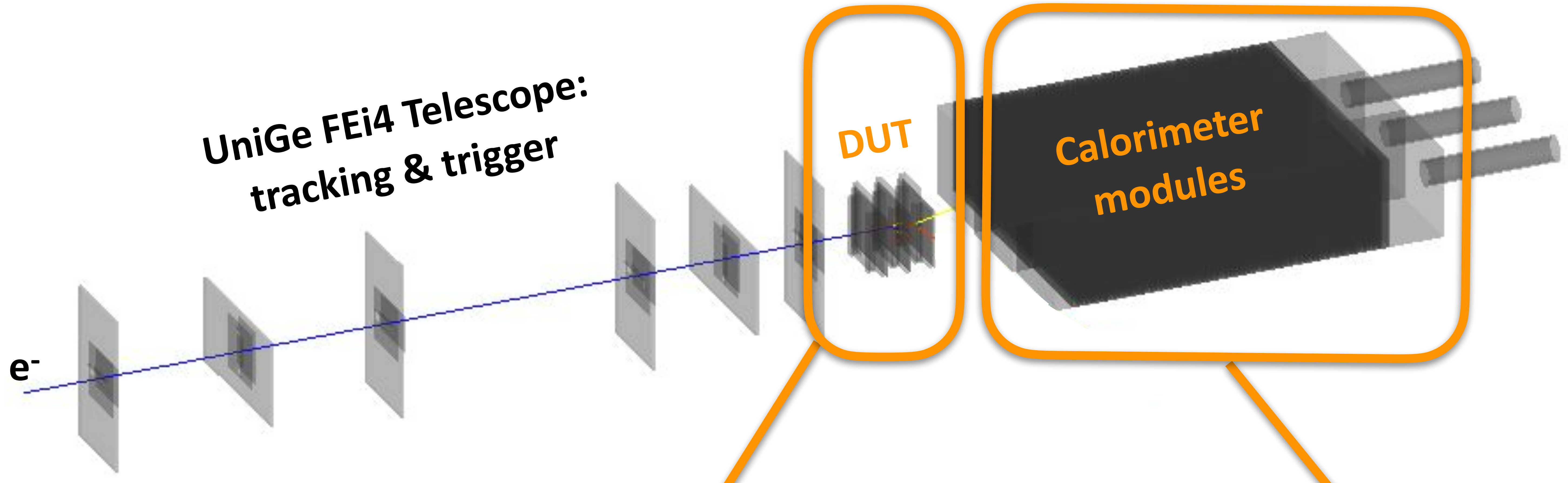

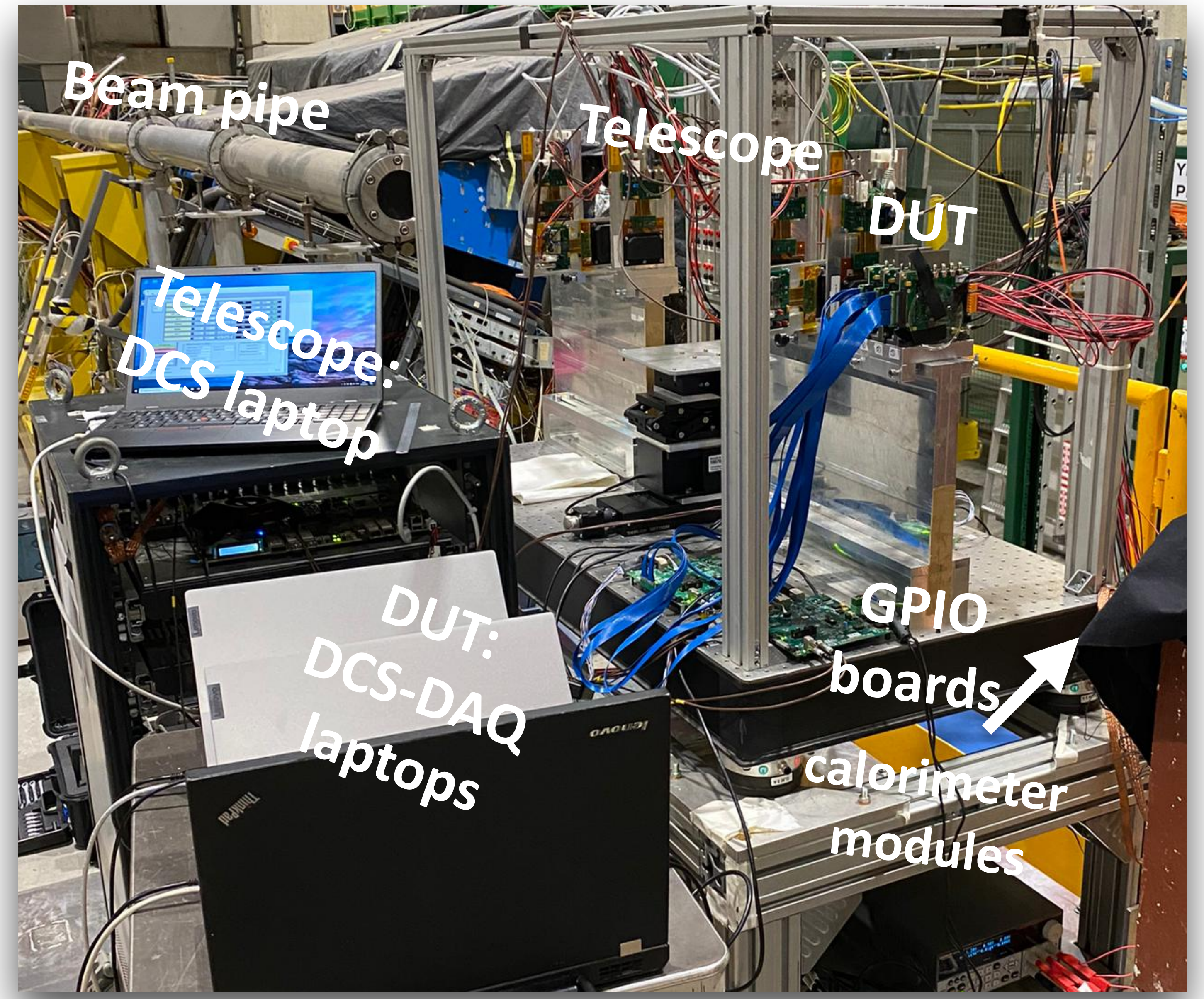

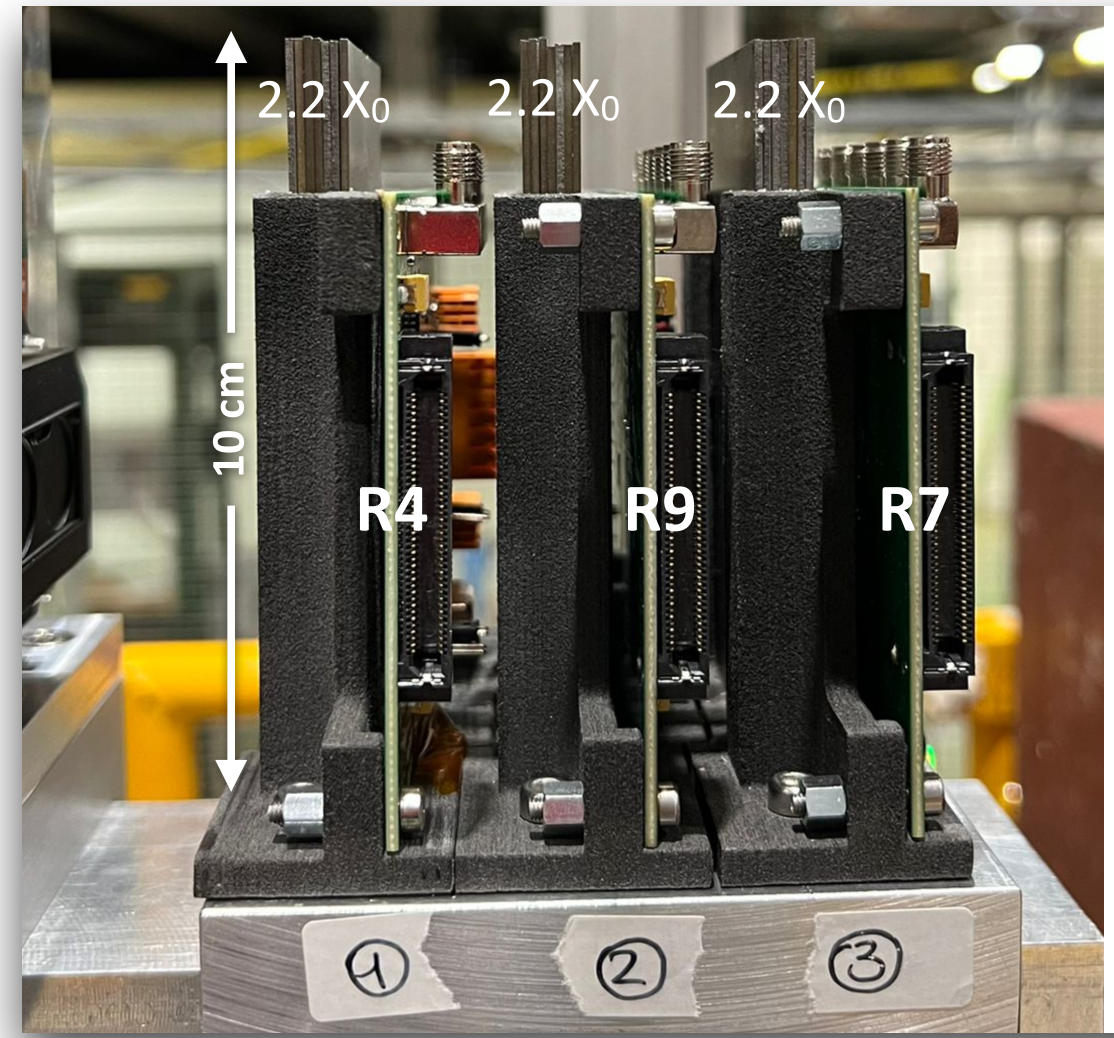

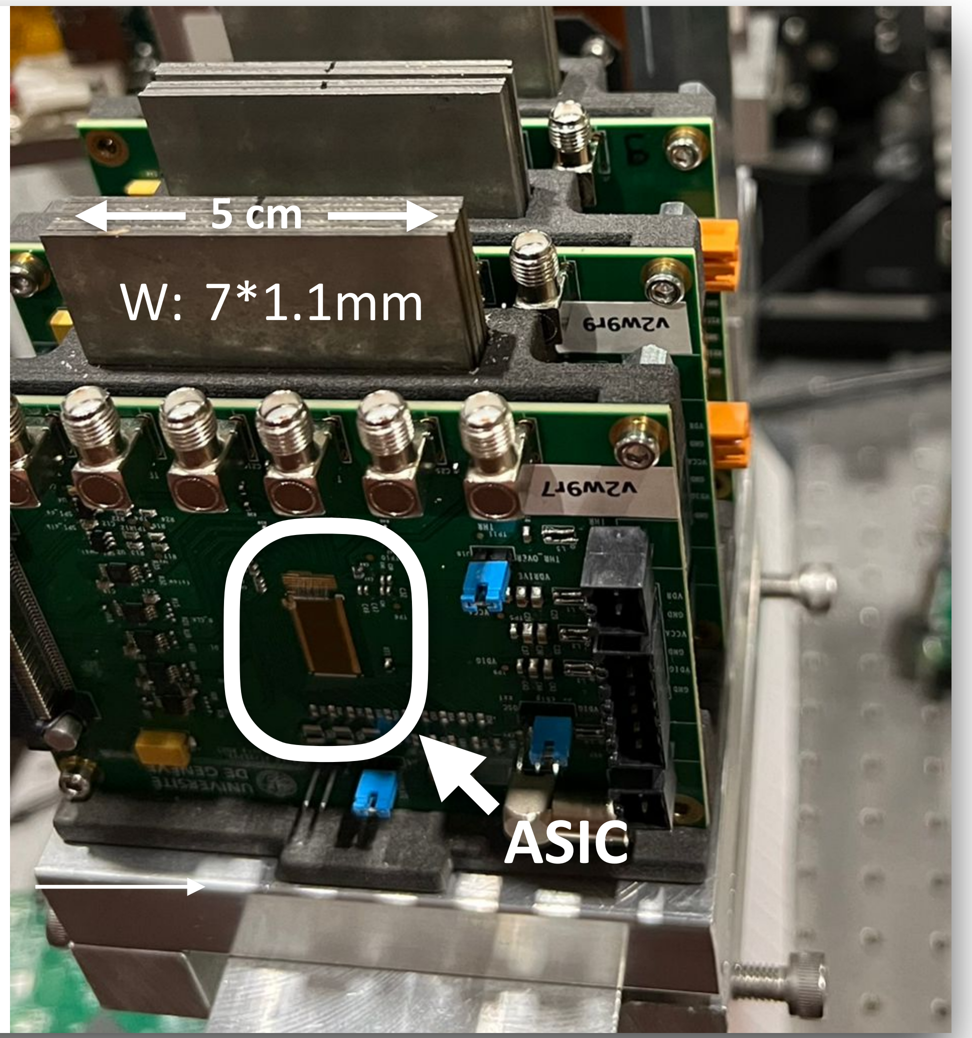

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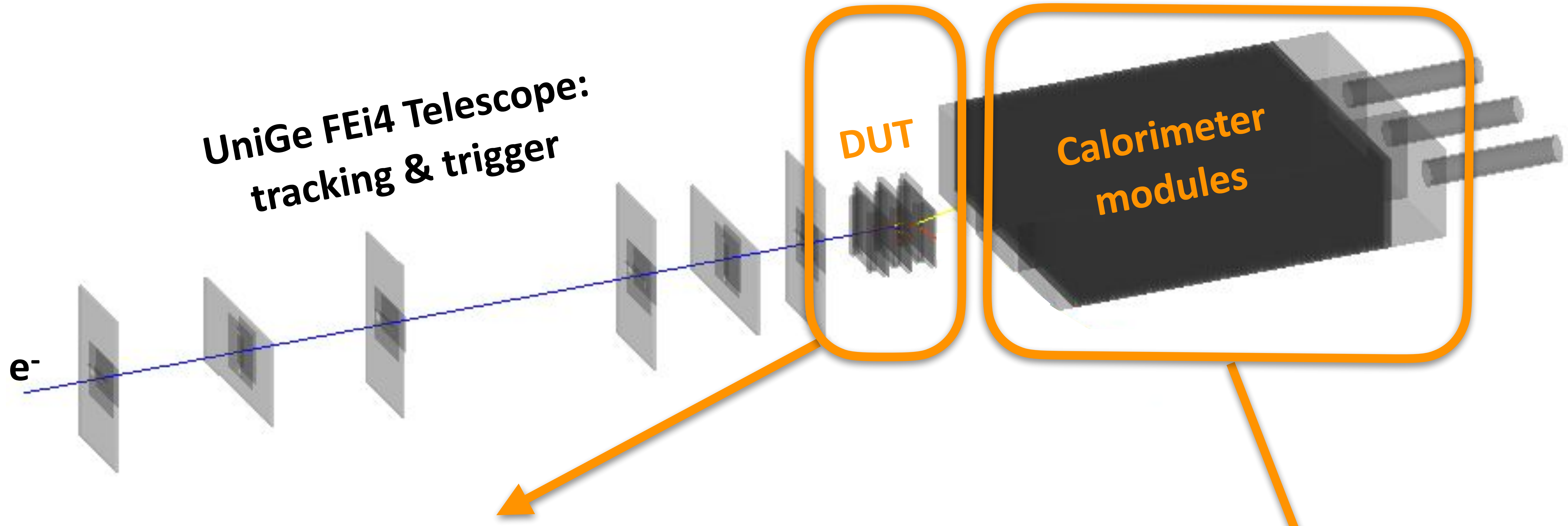

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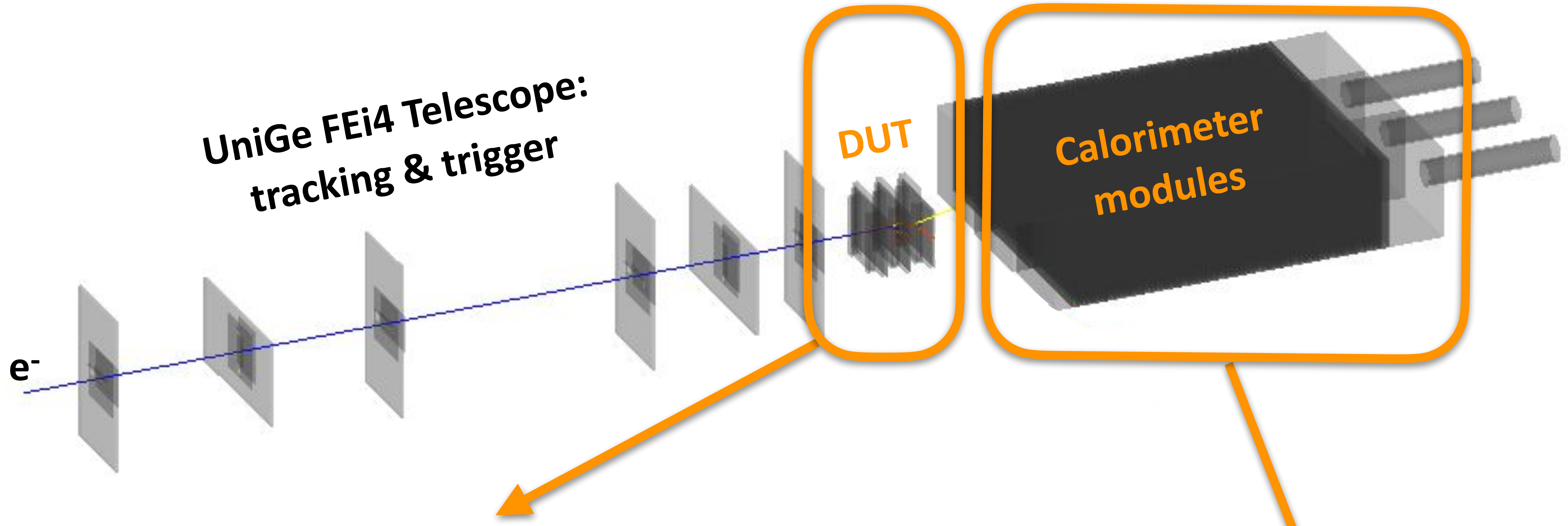

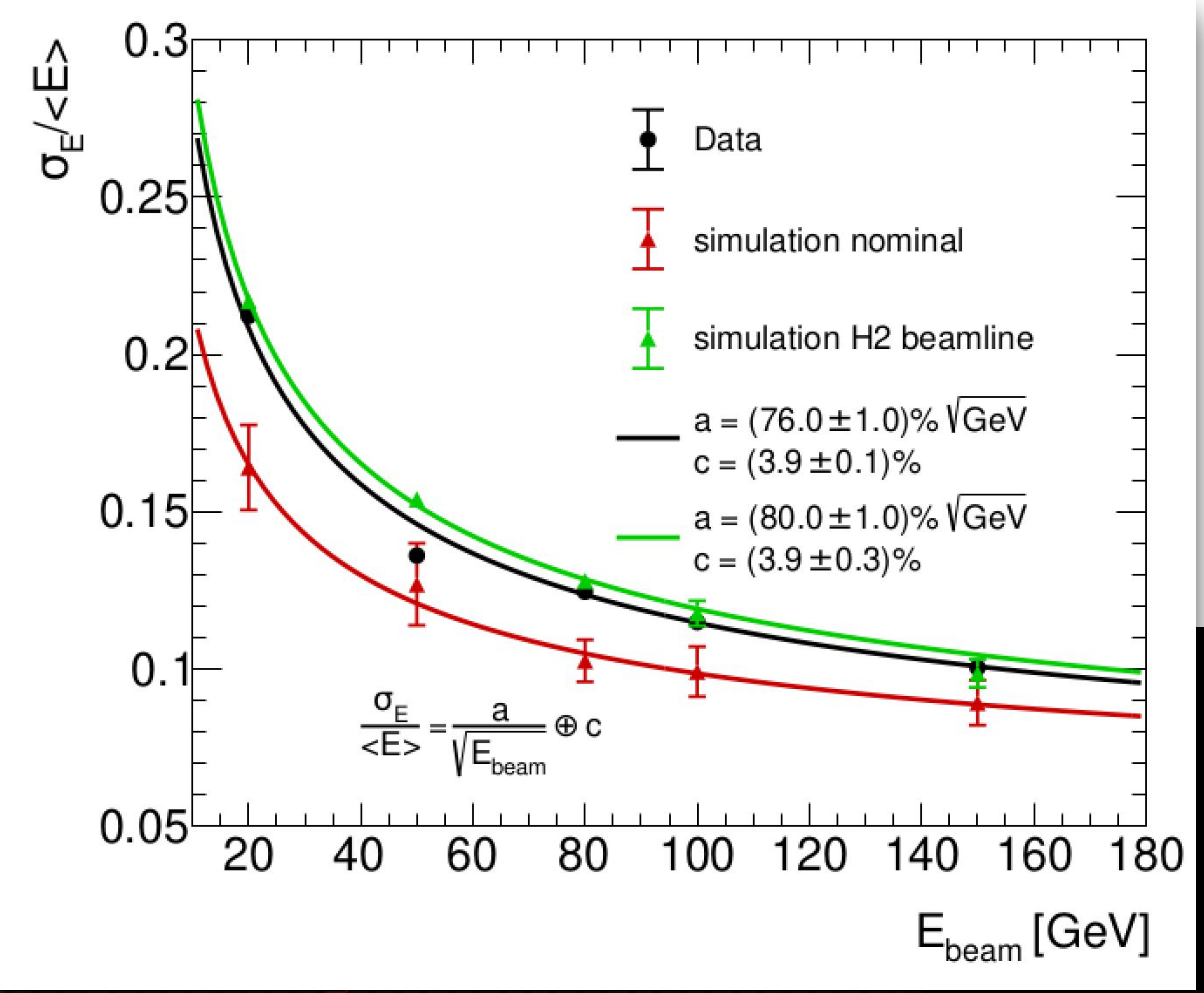

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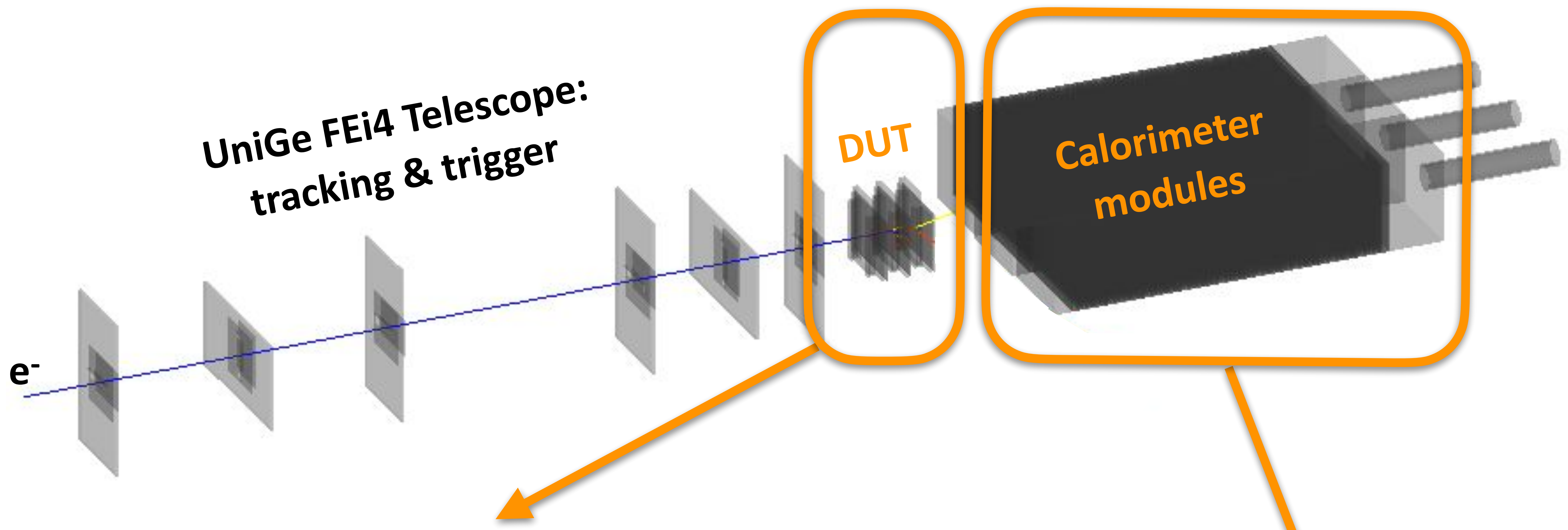
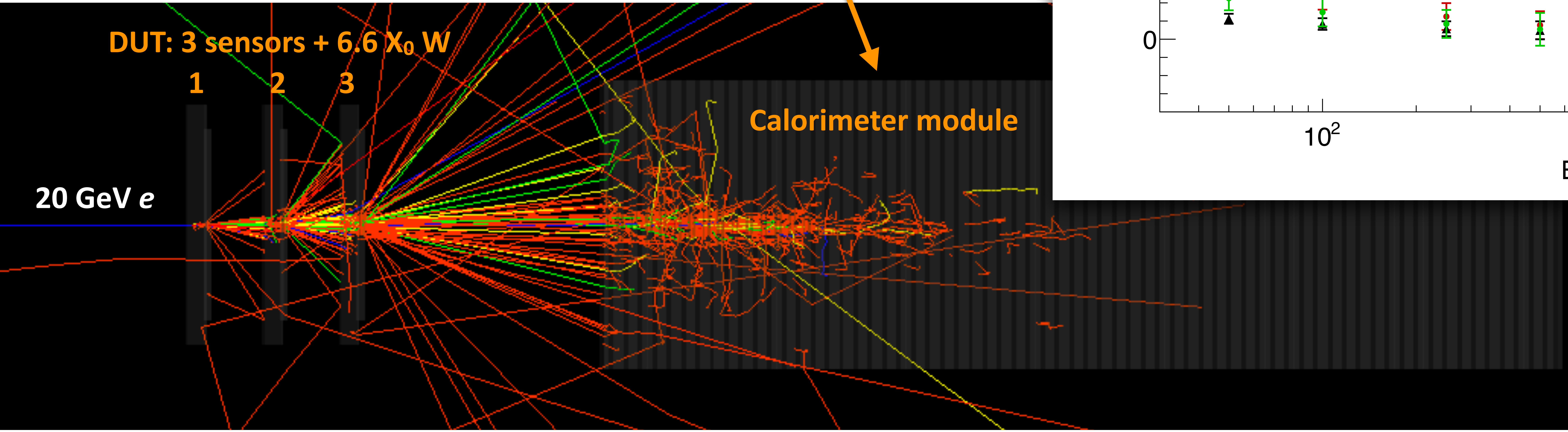
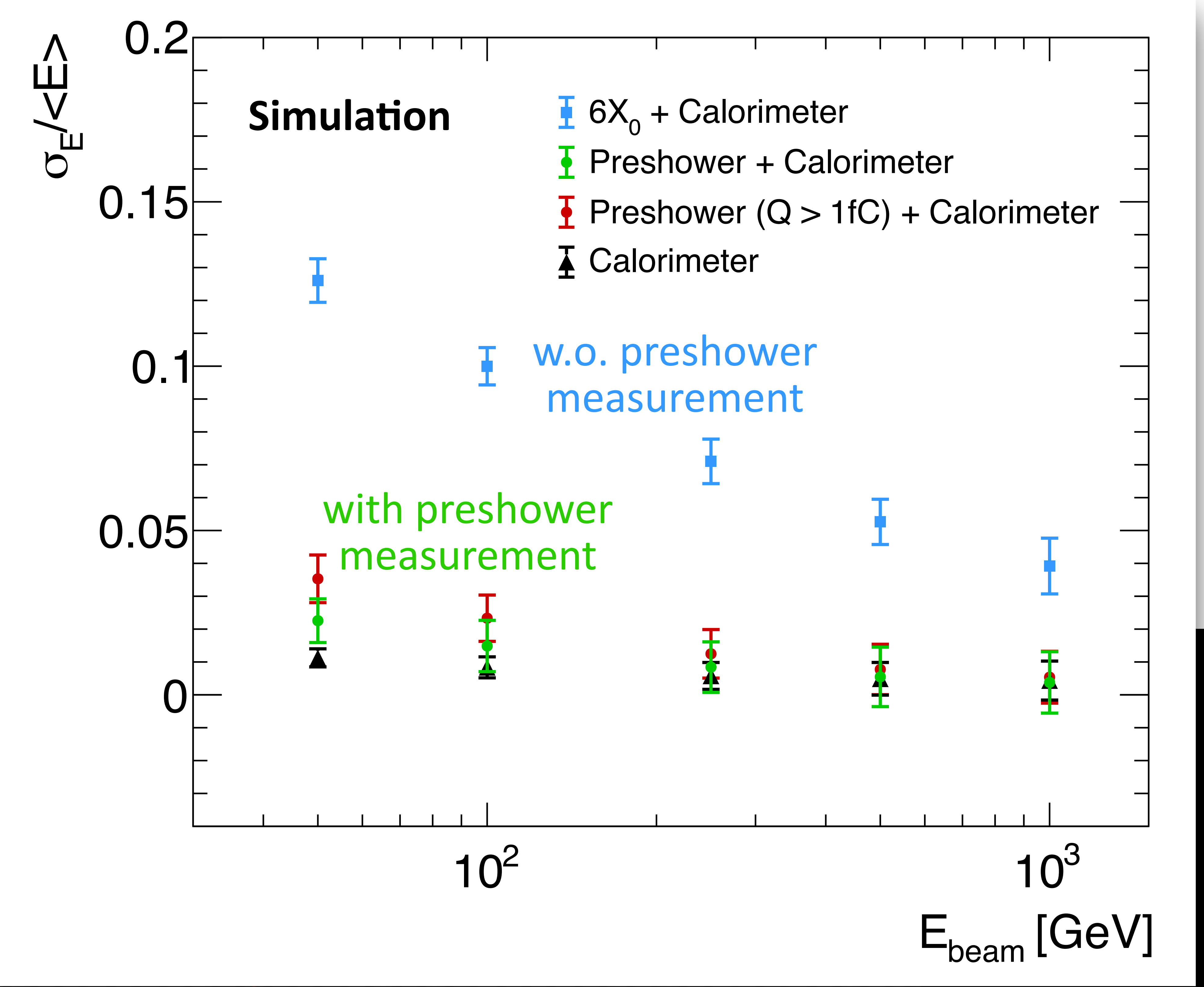
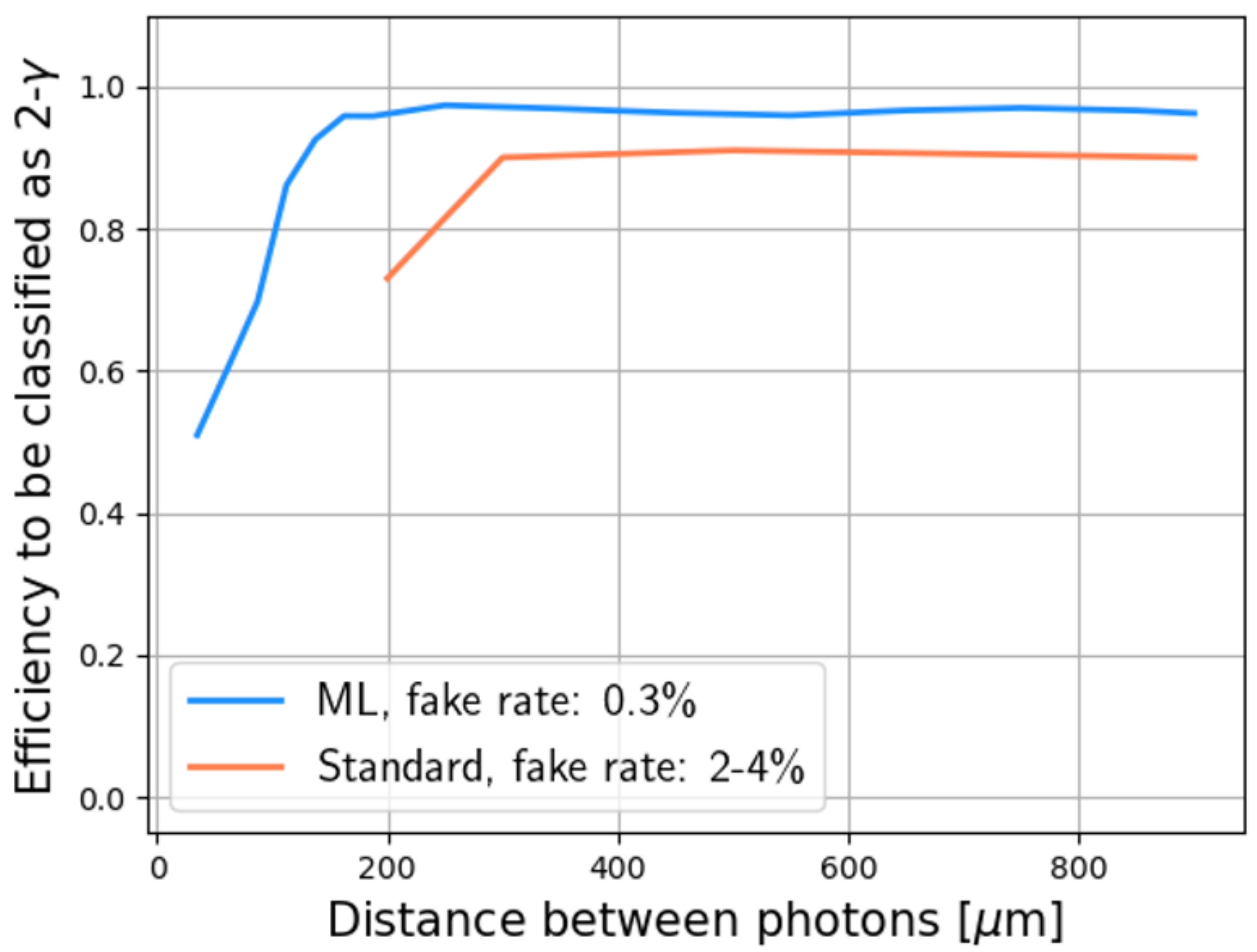


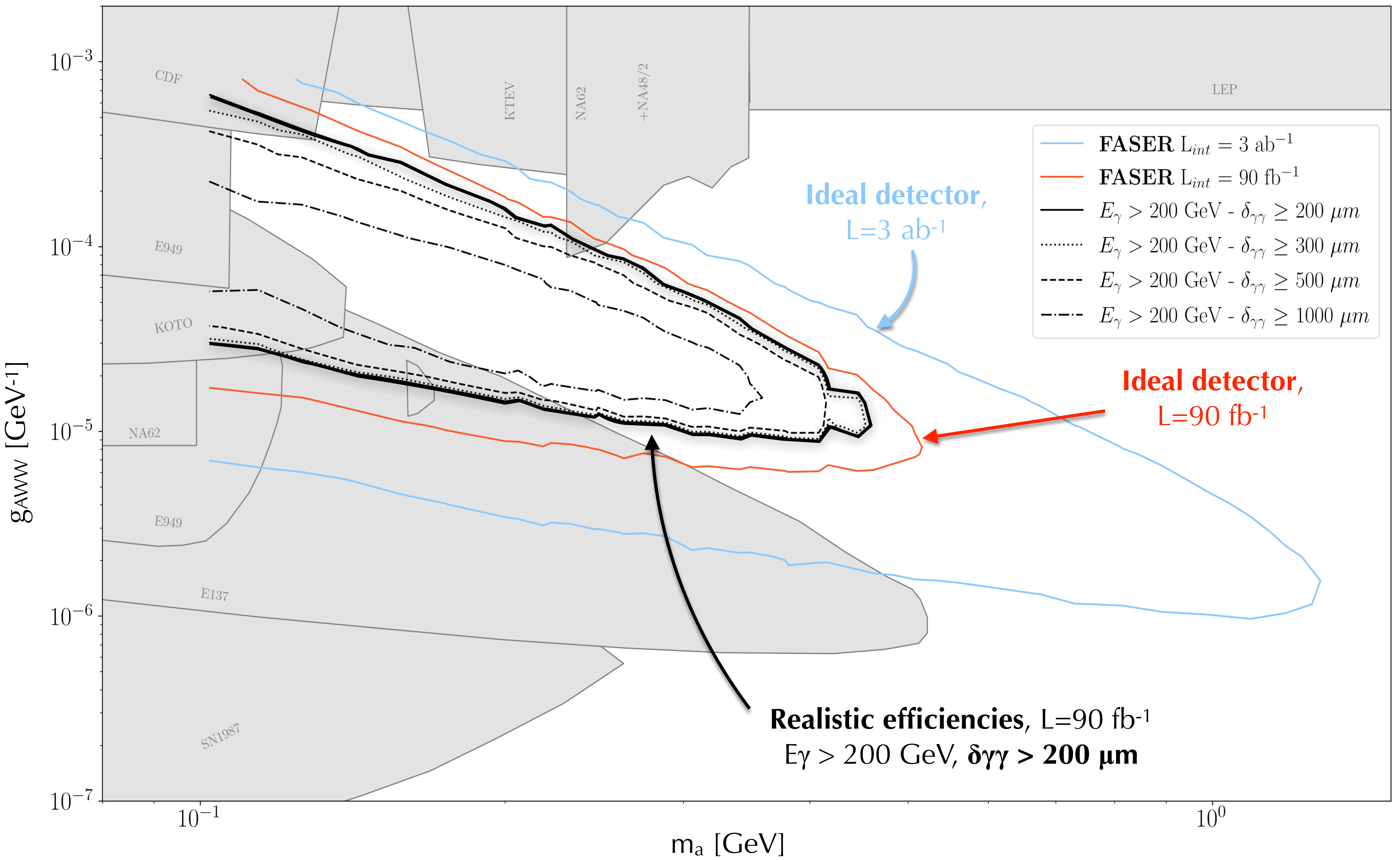




Impact of upgrader preshower evaluated for benchmark dark photon (a) model

- $\mathcal{L} \sim g_{aWW} a W \tilde{W}$ coupling to SU(2)$_L$
- abundant LHC production thanks to coupling with W
- a exclusively decays to $\gamma\gamma$



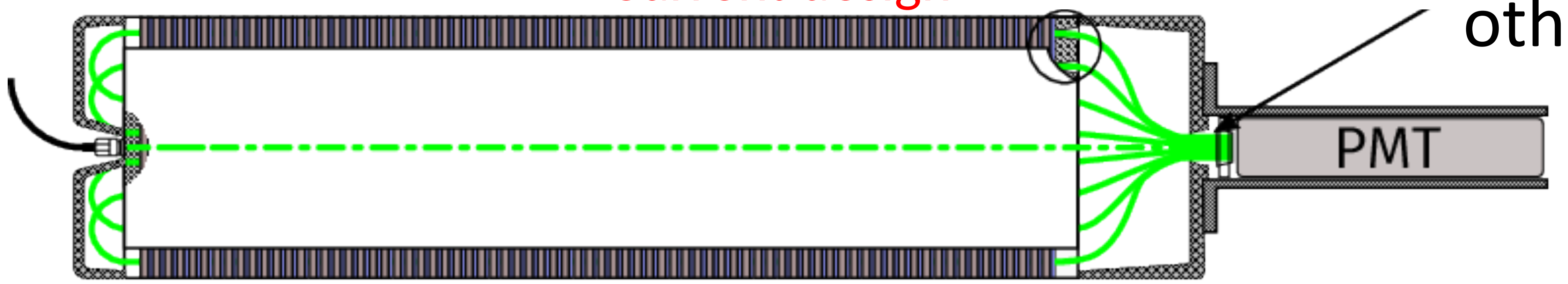


Upgraded Calorimeter Readout Scheme

Plan to upgrade the calorimeter readout scheme to improve *range* and *energy scale*

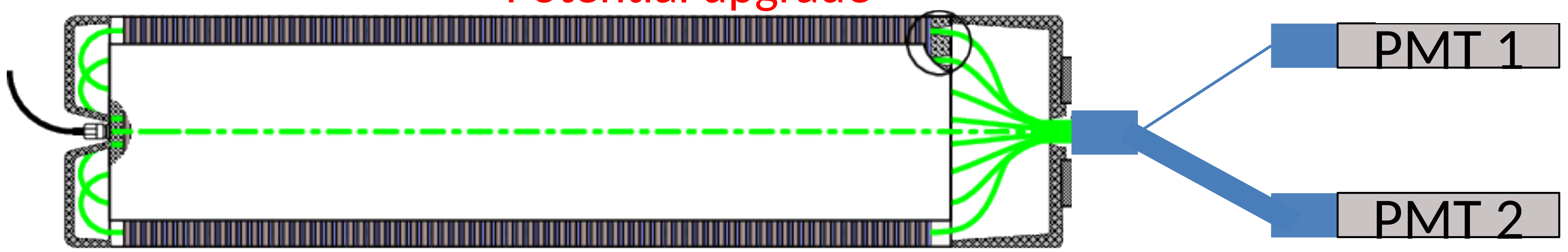
- Currently relying on single PMT, and optical filter to reduce light output by factor 10
  - ↳ *Calibrations: MIP data (high PMT gain) extrapolated to low gain with LED-determined gain ratio*
- Upgrade: use two separate PMTs to cover low E (high gain) and high E (low gain) at same time

Current design



Light output reduced by *optical filter,* otherwise too large signal at TeV scale

Potential upgrade



Upgrade: same PMT type, but operated at medium gain

High energy range PMT: 3-3000 GeV

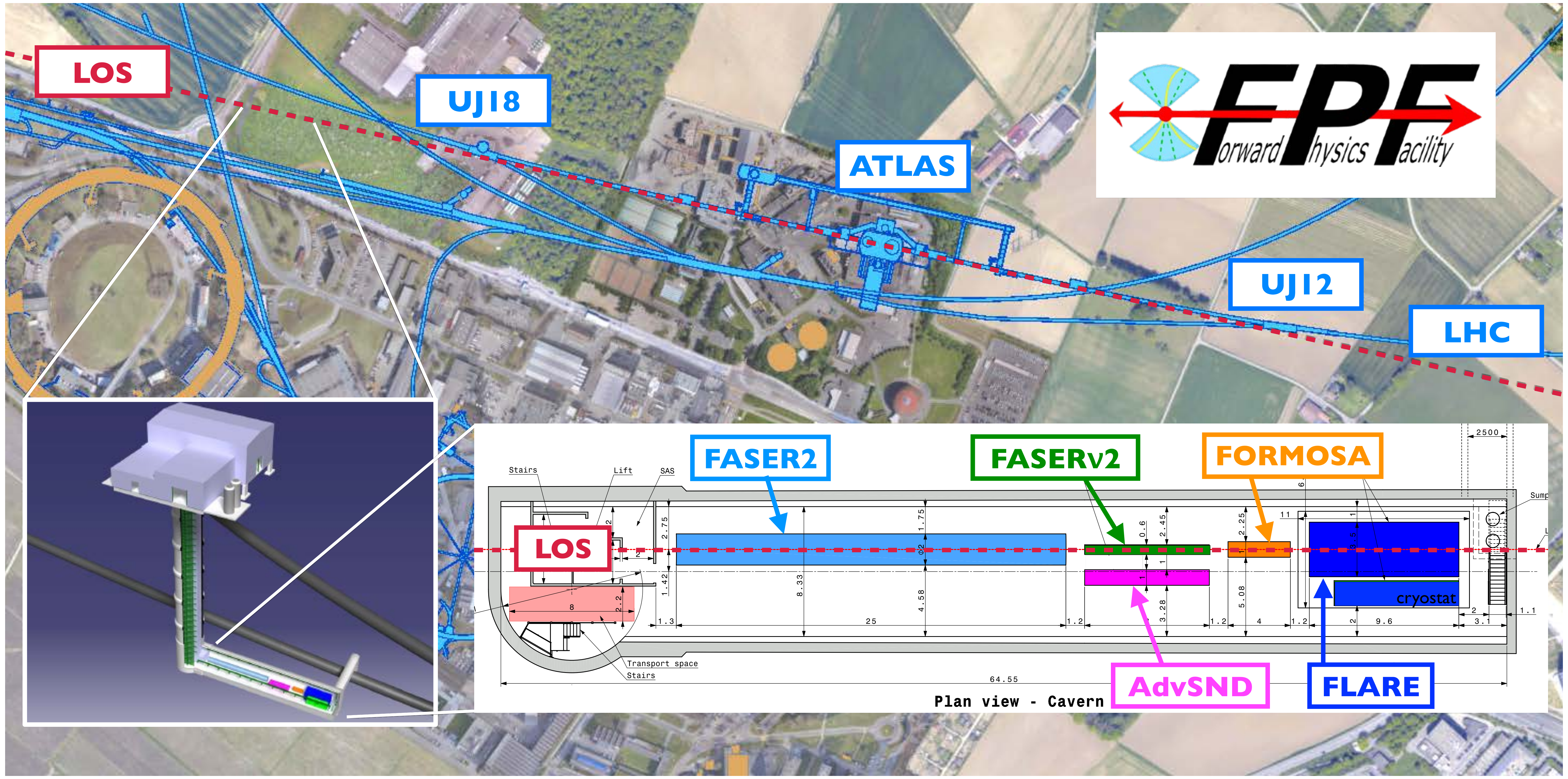
Low energy range PMT: 0.1-300 GeV

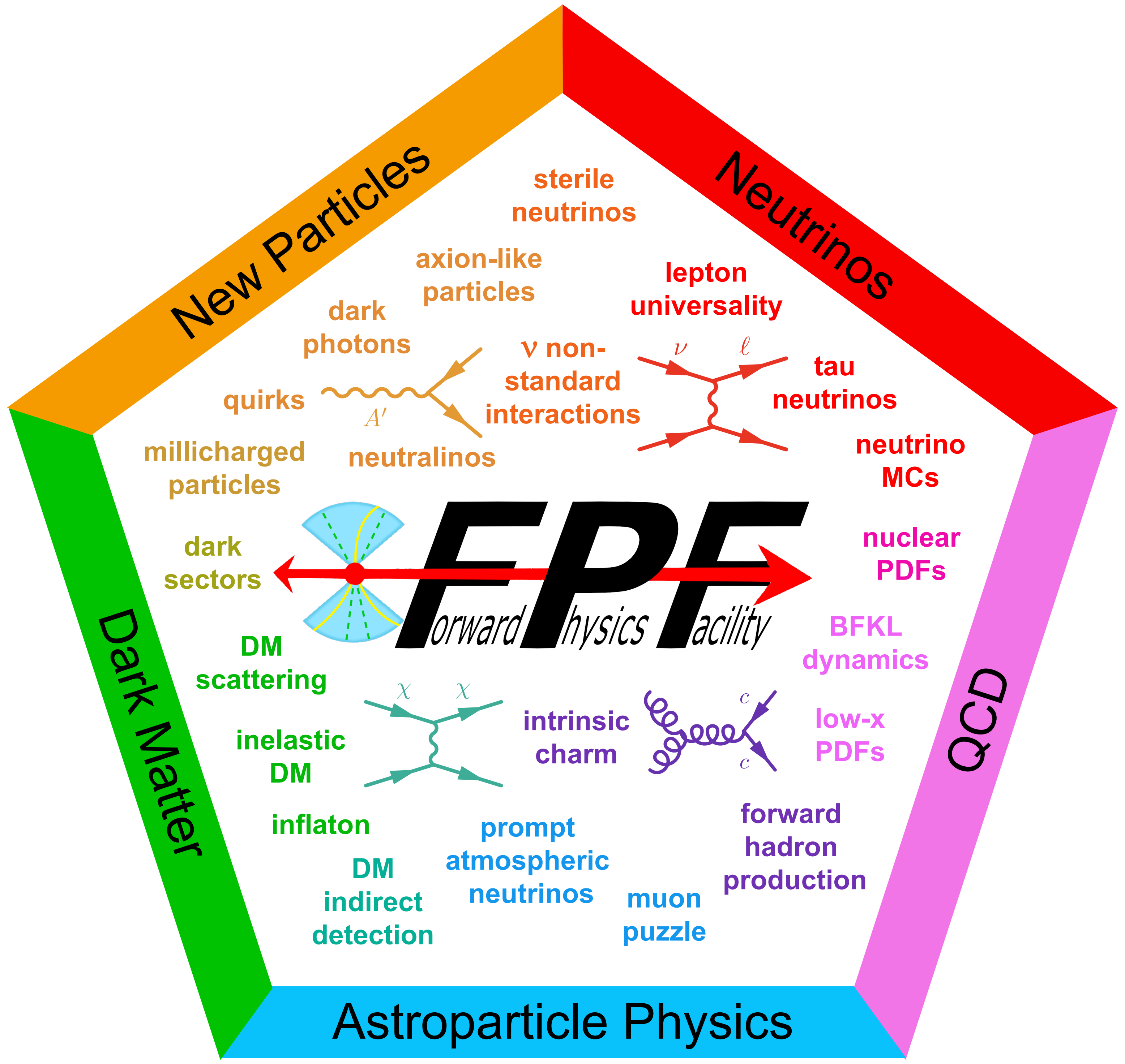
⇒ 3-300 GeV overlap region for cross-calibrations

Proposal [Link]: Forward Physics Facility at the LHC

FASER 2 upgrade proposed in the context of a broader Forward Physics Facility (FPF)

- 65 m long and 9 m wide cavern, 617-682 m west of ATLAS IP, on beam collision axis
- Besides FASER2 and FASERv2, may host several other experiments: FORMOSA, AdvSND, FLArE, …

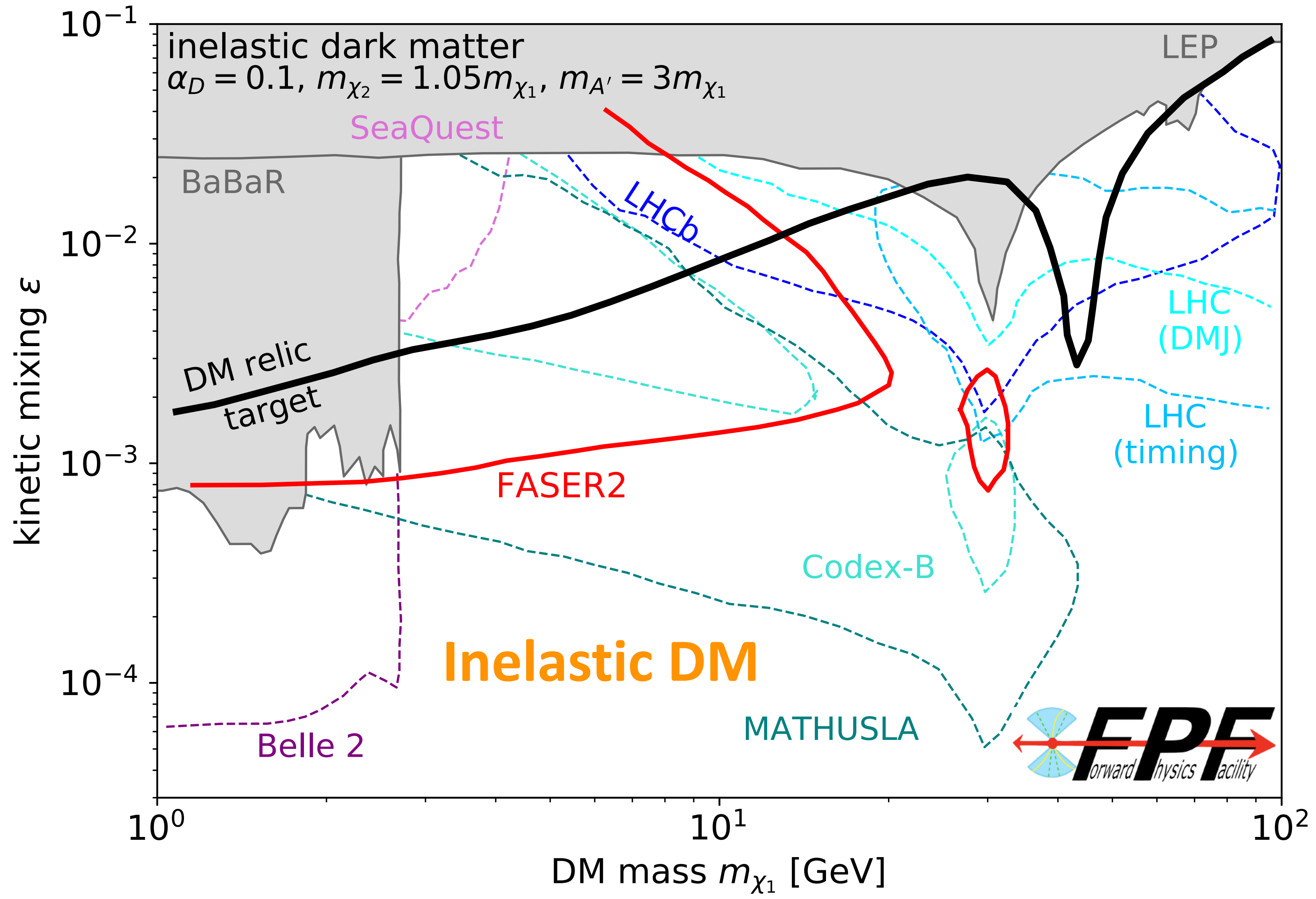


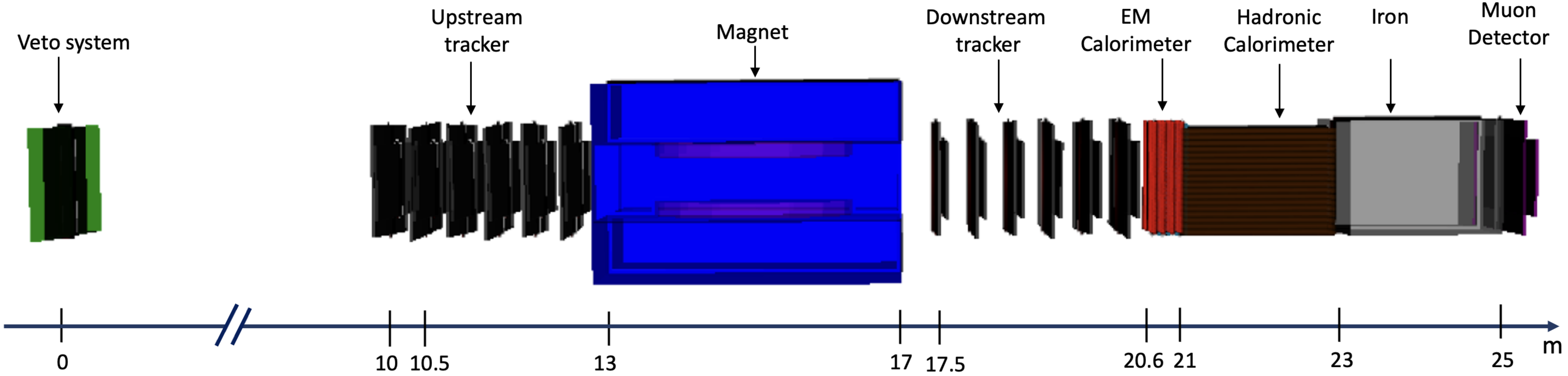


FASER2 And FASERν2

FASER2 detector: wider, and longer

- π^0 angular acceptance increasing from 0.6% to 10%
- Improved sensitivity to large LLP masses and longer lifetimes
- Larger volume requires revised instrumentation strategy:
  - ↳ *need 4 Tm bending power: superconducting magnets*
  - ↳ *much bigger tracker: silicon (mostly) replaced by SciFi*

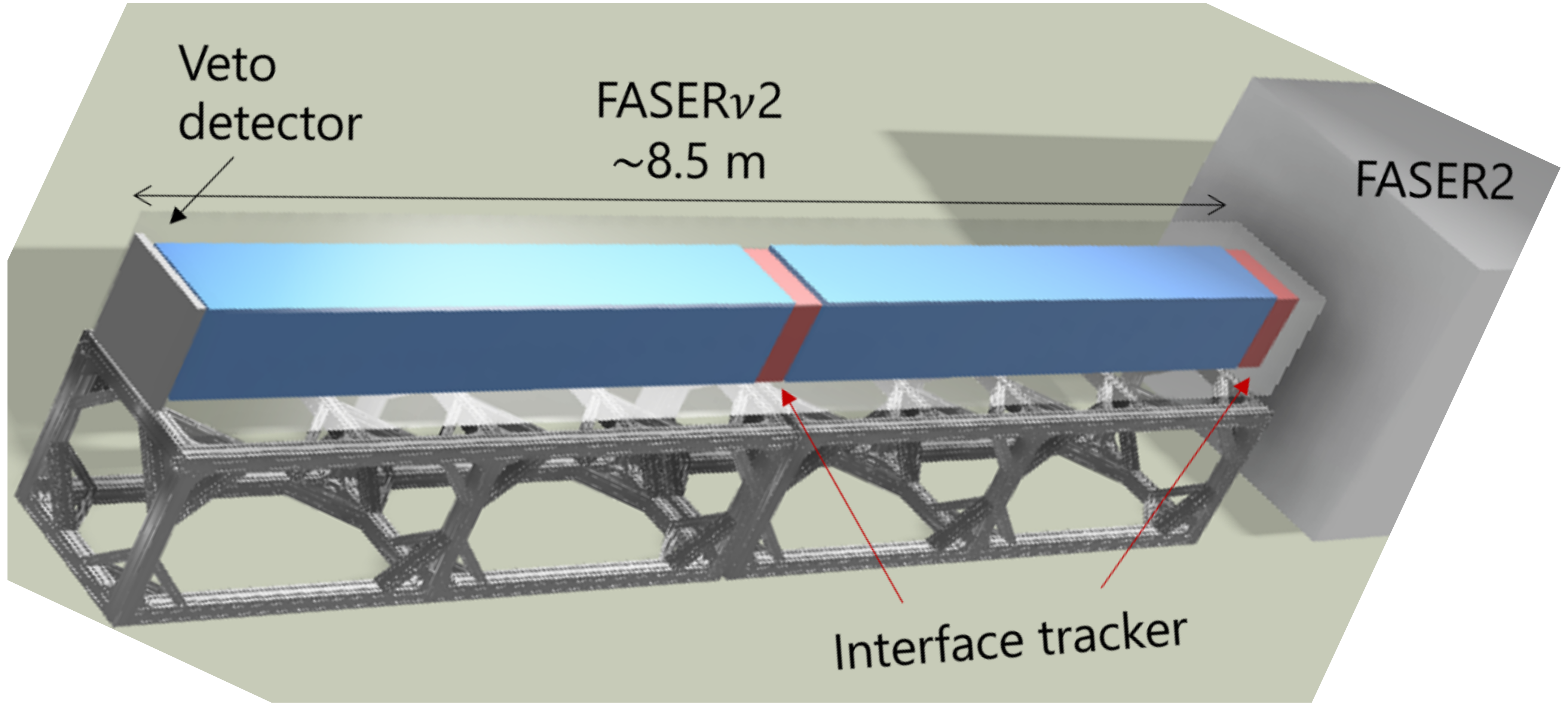


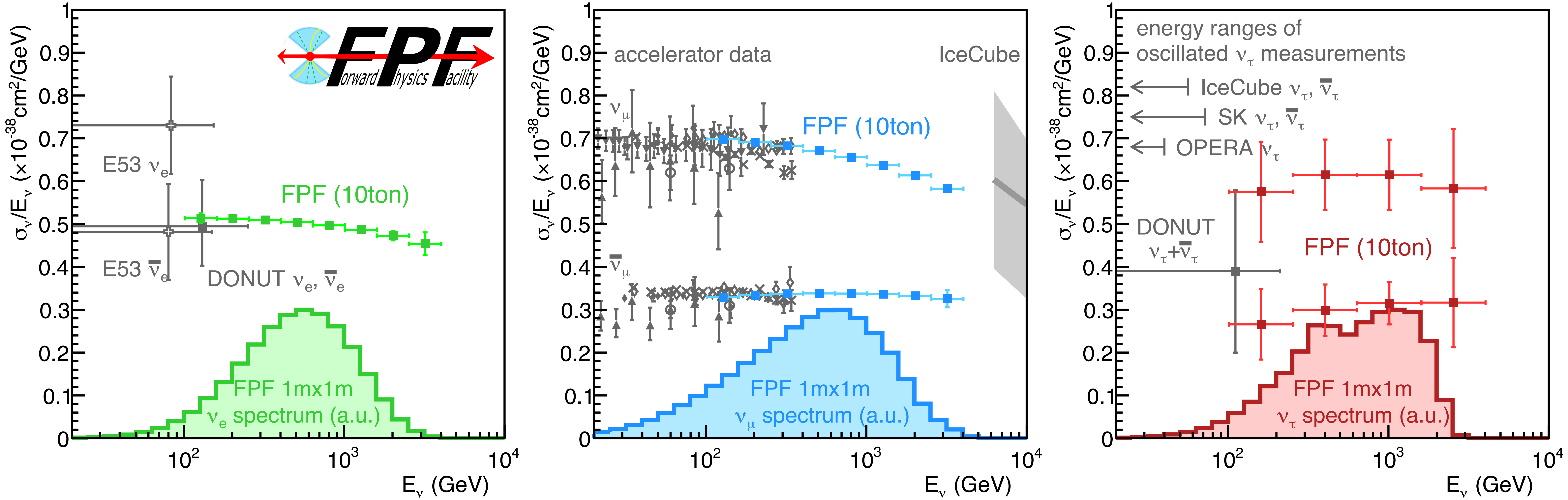


FASER2 And FASERv2

FASERν2: 20-ton emulsion-based ν detector

- 3300 AgBr layers interleaved with tungsten plates
- veto + two tracker planes to interface with FASER2
  - ↳ *μ charge, and global event reconstruction*
- for HL-LHC, expect: $O(10^6)$ ν_μ, $O(10^5)$ ν_e, $O(10^4)$ ν_τ





Summary & Outlook

Empowering FASER's capabilities with several upgrades…

- **New preshower will enable multi-γ tagging and greatly increase dark photon searches' reach**
  - ↳ Detector layout and mechanics design converged; pre-production ASIC extensively tested
  - ↳ Final chip design just submitted to foundry: targeting preshower installation in 2024
- **Calorimeter readout scheme upgrade: extended range and improved energy scale**
- **Further upgrades proposed in the context of a broader Forward Physics Facility**
  - ↳ Wider and longer FASER2 detector to tackle larger LLP masses and longer lifetimes
  - ↳ Bigger and more complex FASERv2 system to expand neutrino physics program

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… Many years of exciting physics ahead of us!

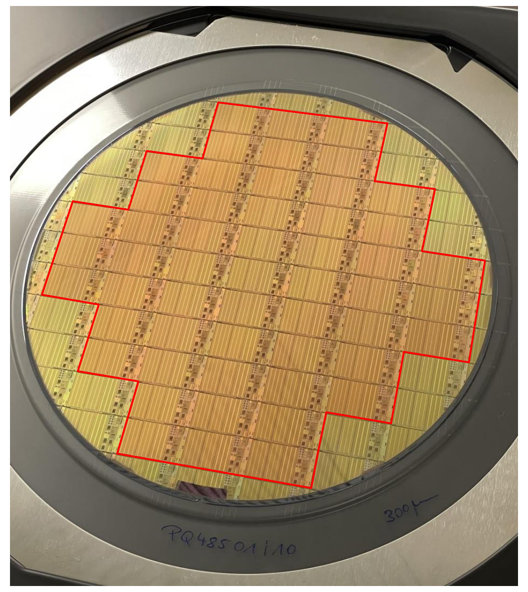
Spares

Pre-production ASIC Prototype: Tests

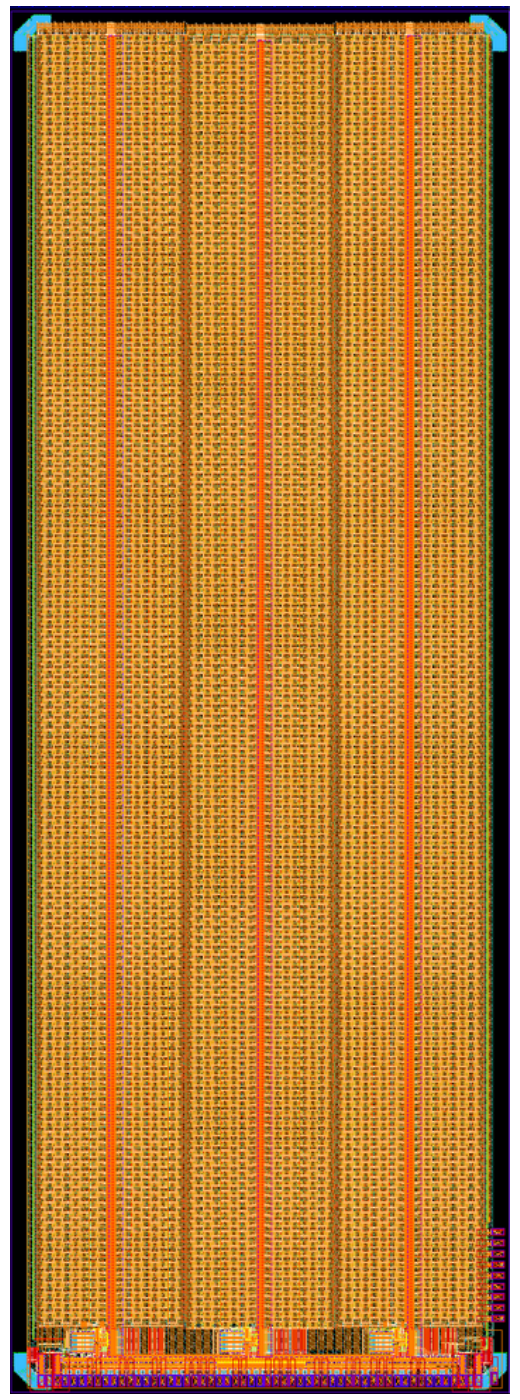
Reticle: 2.4 x 1.5 cm^2

53 reticles per wafer

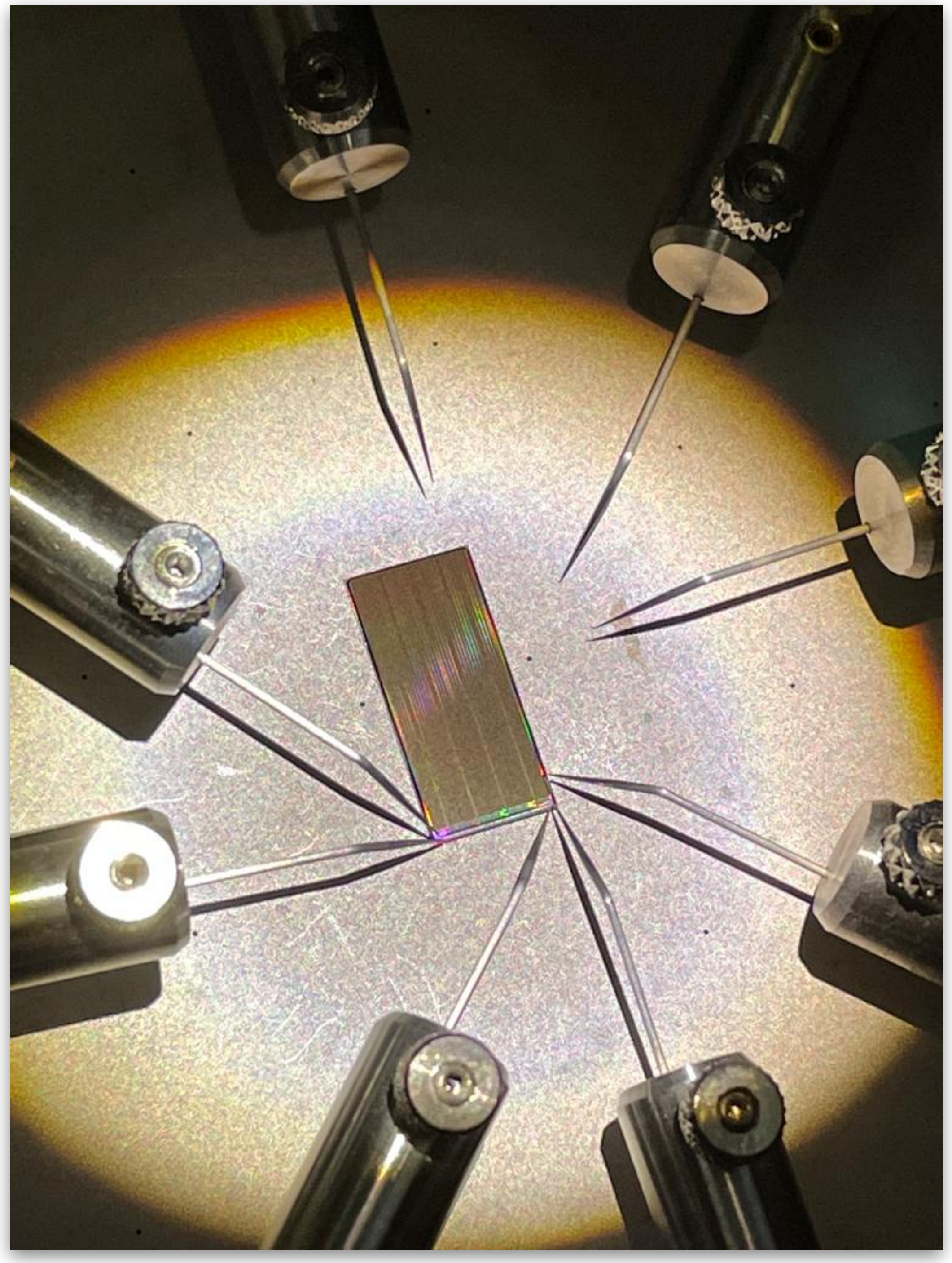
Thickness 300 µm



CHIP Schematic

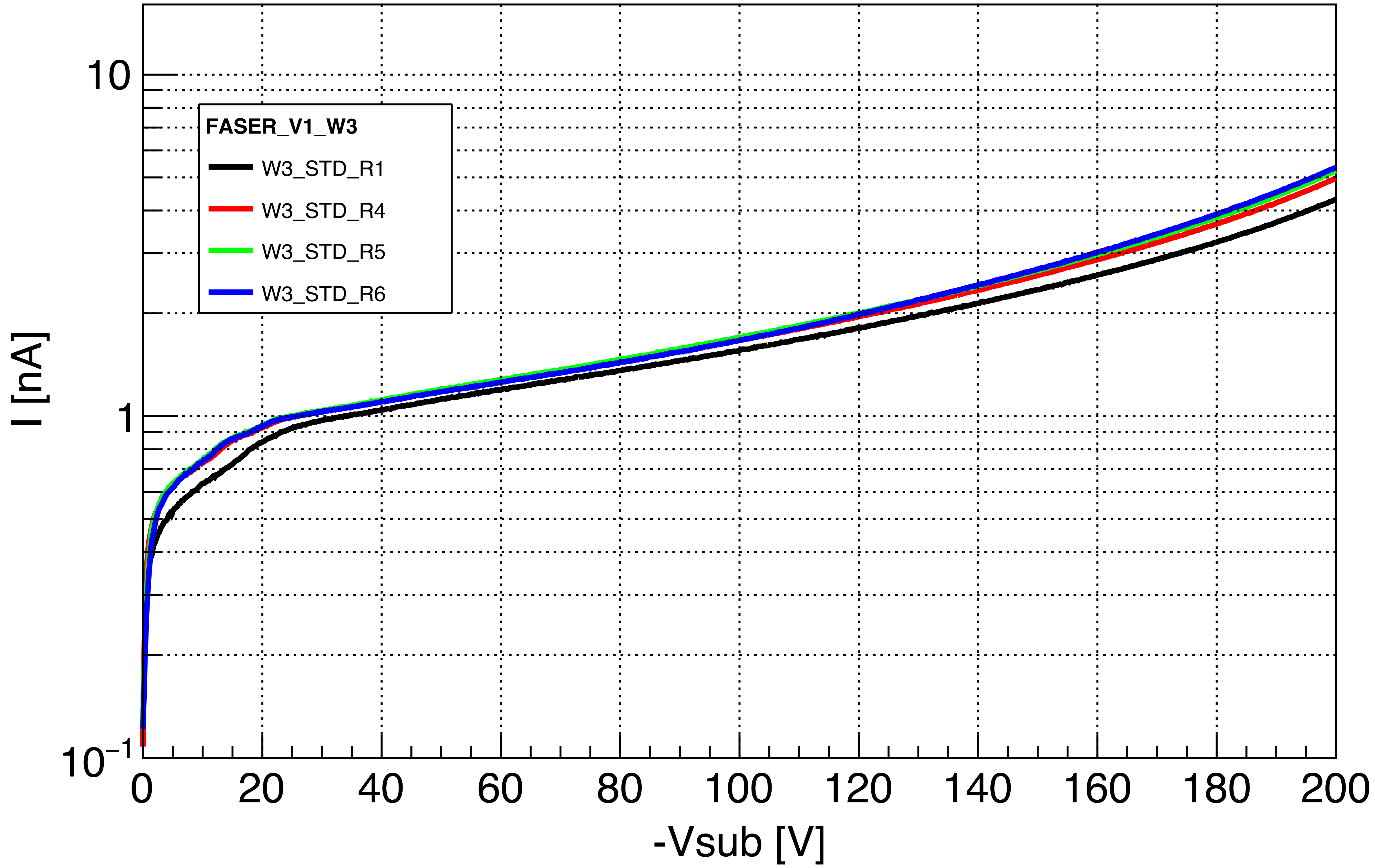


CHIP @ probe station



Wafers received in Jun 2022, tested in laboratory

- I-V characteristics measured at probe station
- Charge response scrutinised with ^{109}Cd and IR laser
- Stress-tests for digital electronics and readout

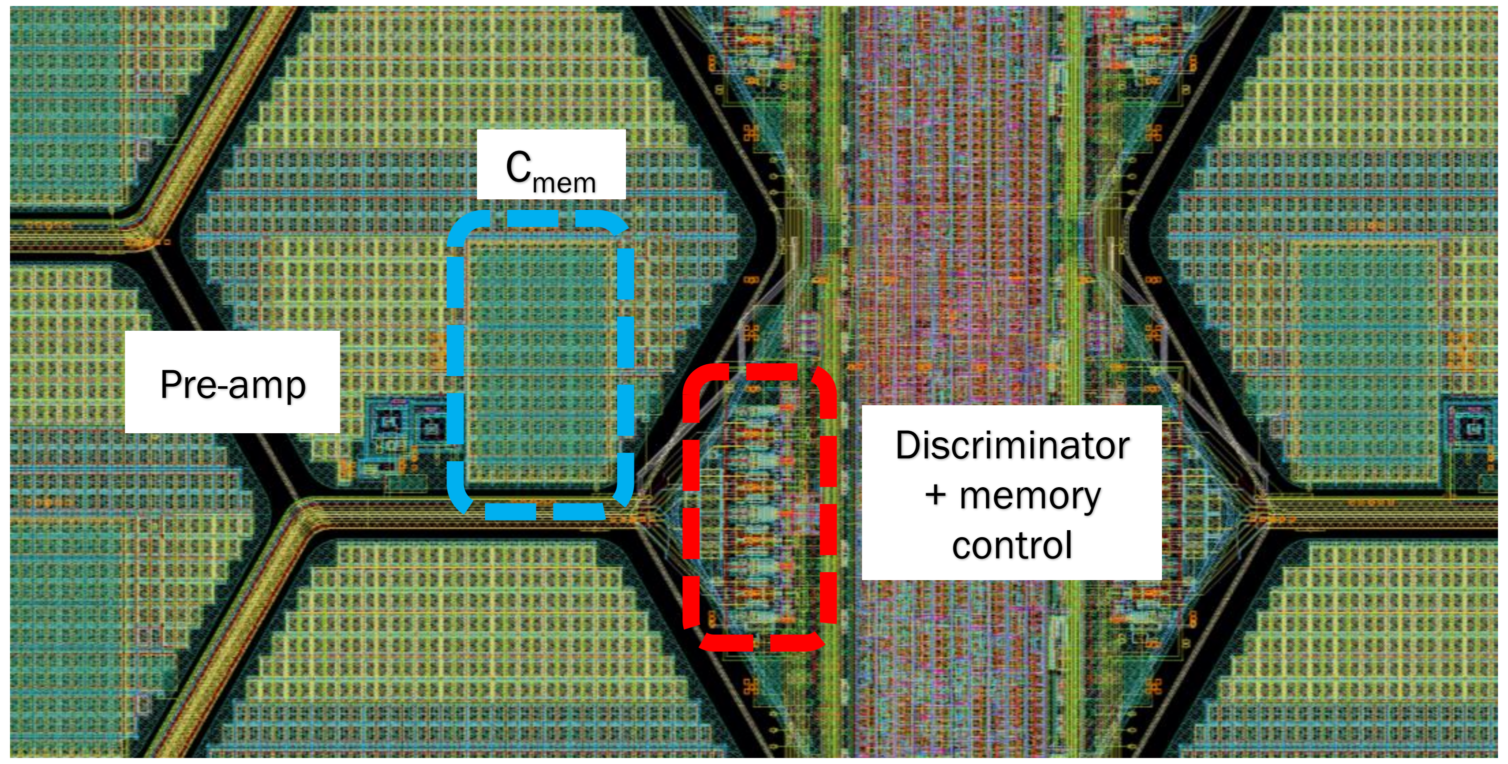


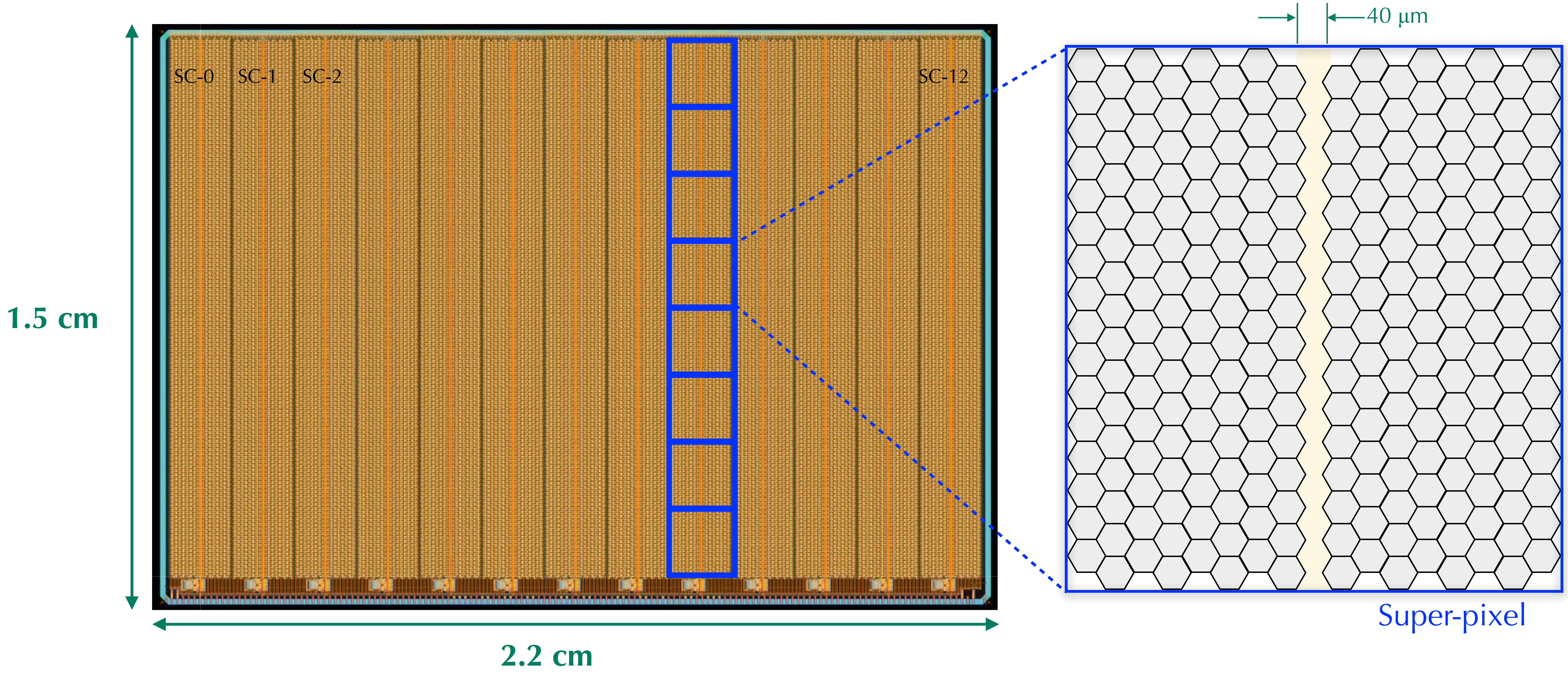
Monolithic Pixel ASIC: Chip Structure

Chip organized in 13 "*super-columns*", each with:

- active region, subdivided into 8 "*super-pixels*" of 16x16 pixel each
- digital column (40 μm) in the middle: sharing of digital electronics

Digital periphery on the bottom, and multiple guard-ring structure





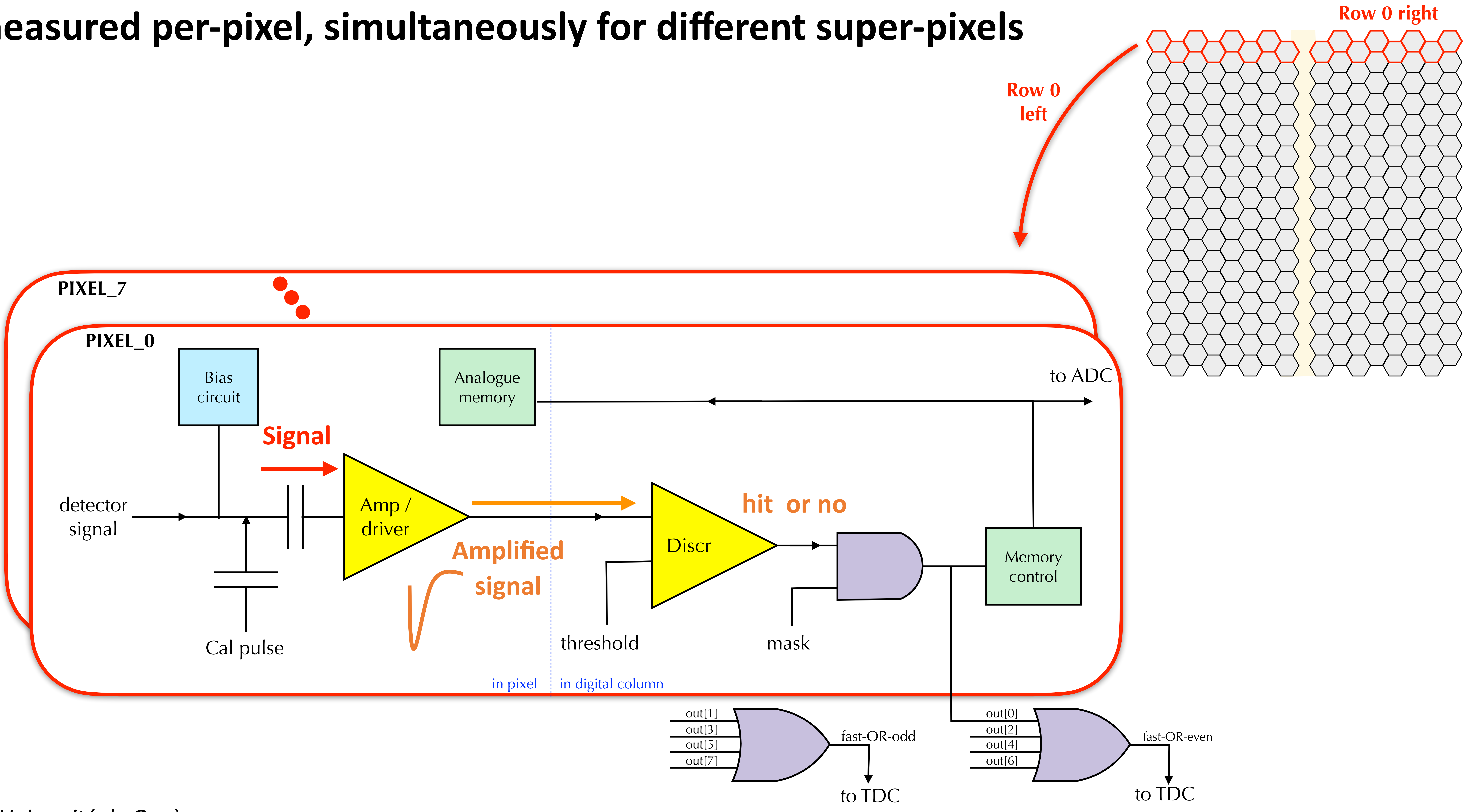
Super pixel:

- 16 rows of 8+8 pixels
- analog multiplexer
- 4-bit flash ADC
- 3 fast-OR lines
- local bias circuit
- programming logic to mask pixels

Dead area <5%

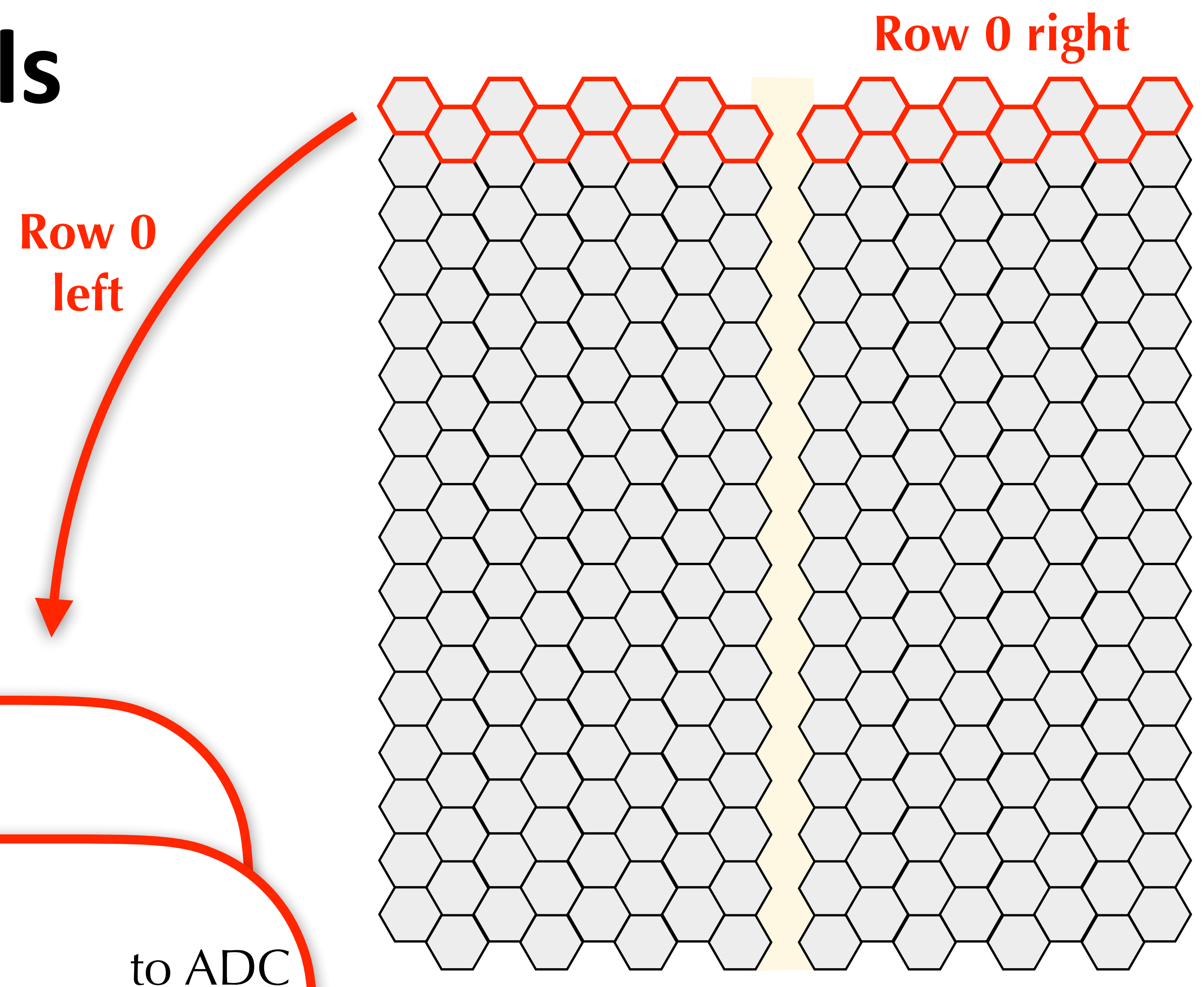
Monolithic Pixel ASIC: Pixel Circuitry

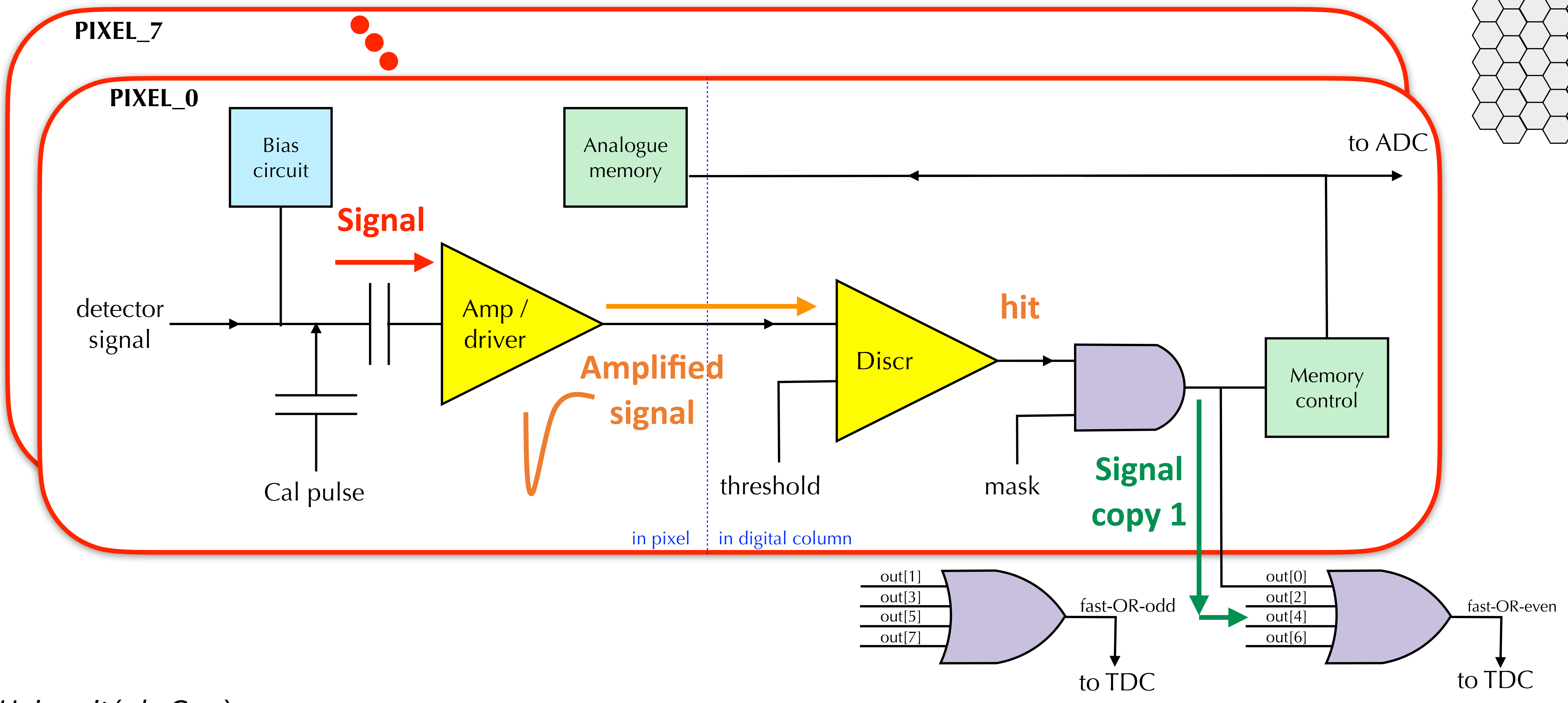
Charge measured per-pixel, simultaneously for different super-pixels



Charge measured per-pixel, simultaneously for different super-pixels

=▶ hit above threshold generates signal sent to periphery via fast-OR

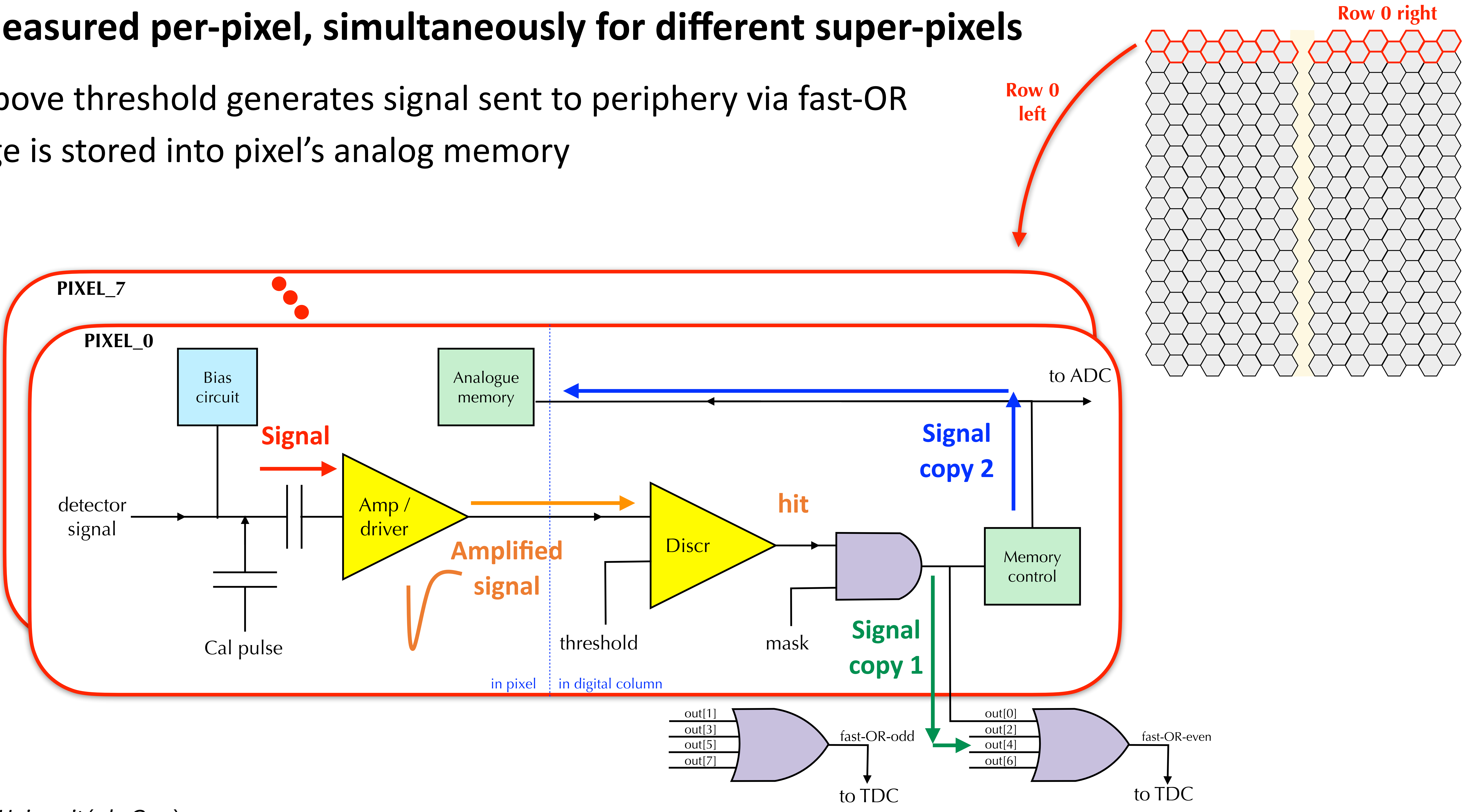




Monolithic Pixel ASIC: Pixel Circuitry

Charge measured per-pixel, simultaneously for different super-pixels

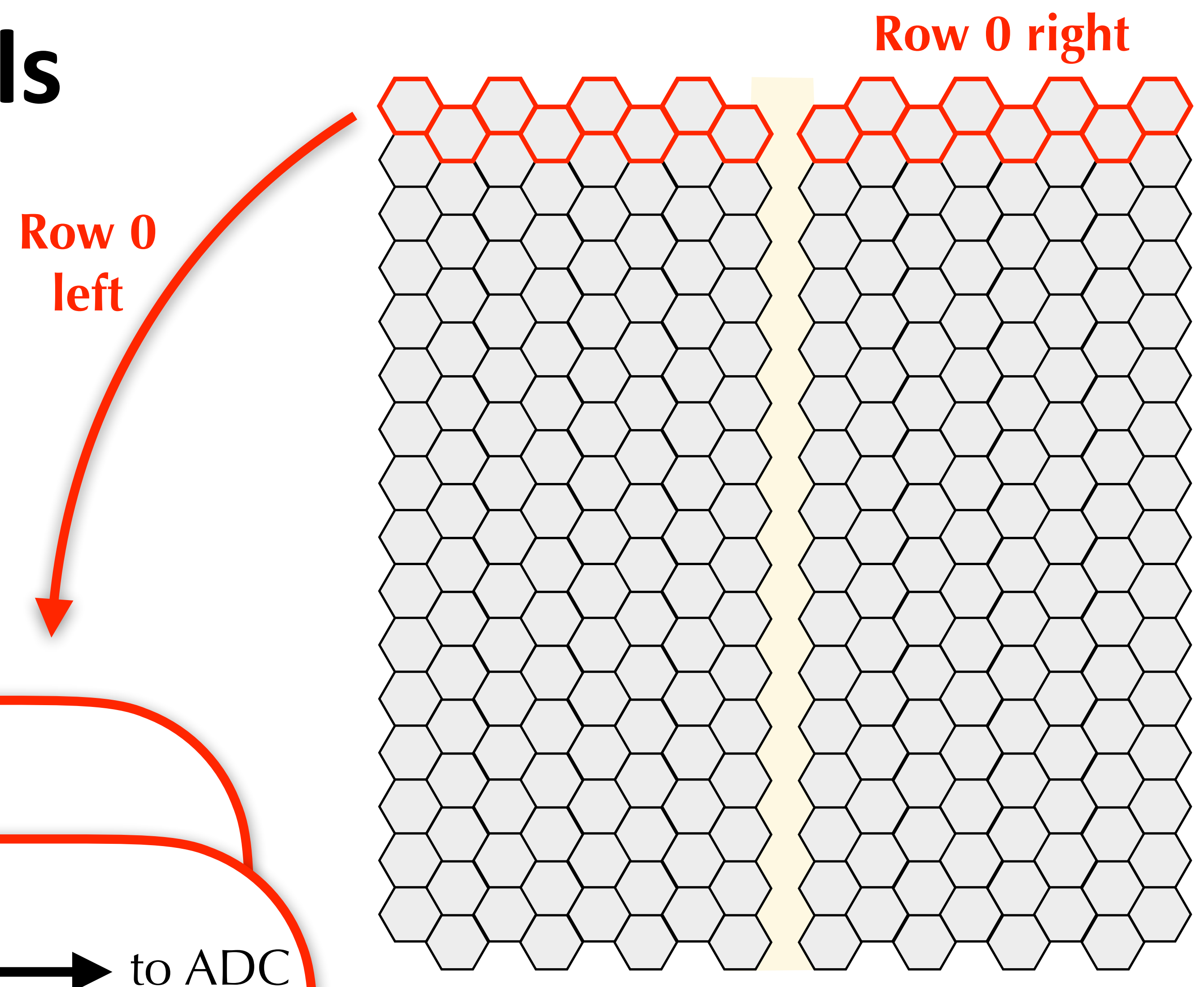
- hit above threshold generates signal sent to periphery via fast-OR
- charge is stored into pixel's analog memory

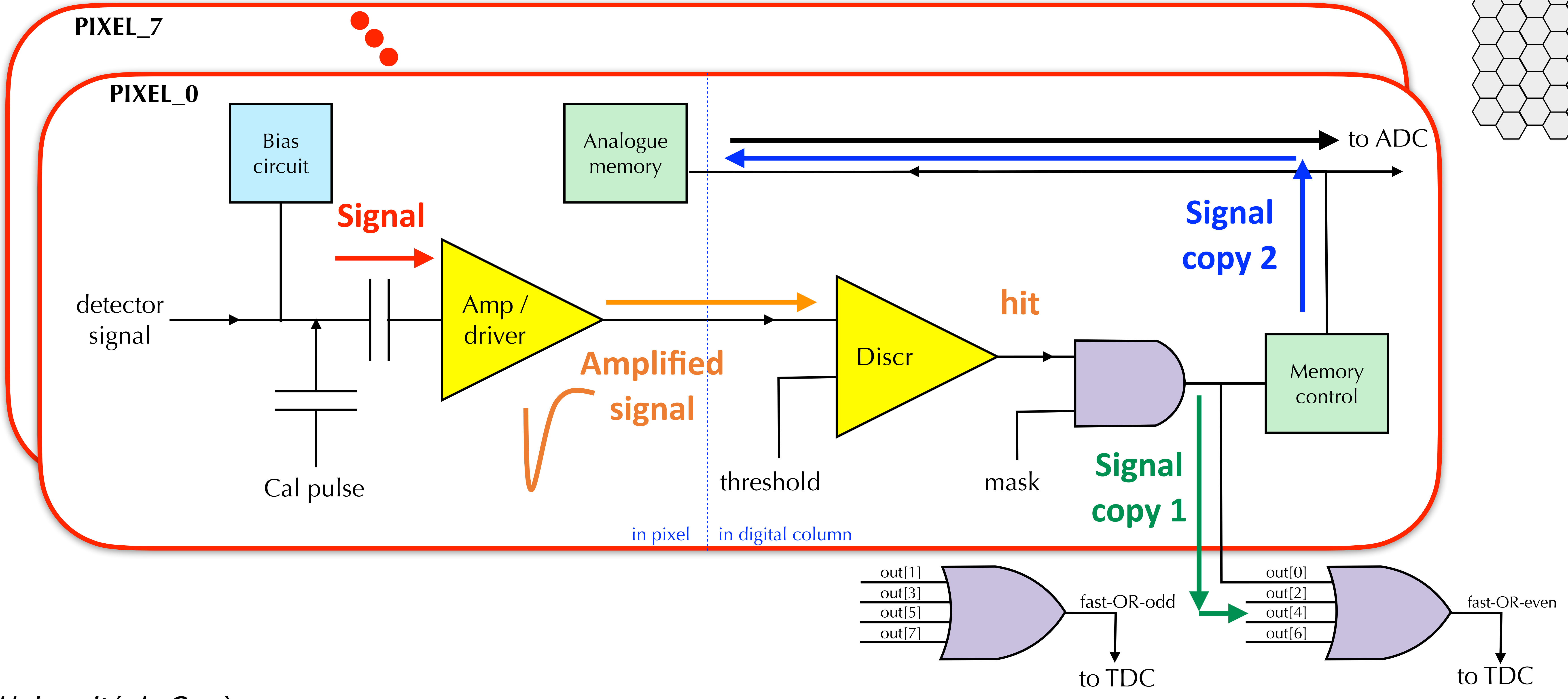


Monolithic Pixel ASIC: Pixel Circuitry

Charge measured per-pixel, simultaneously for different super-pixels

- => hit above threshold generates signal sent to periphery via fast-OR
- => charge is stored into pixel's analog memory
- => after some delay, readout starts super-column after super-column



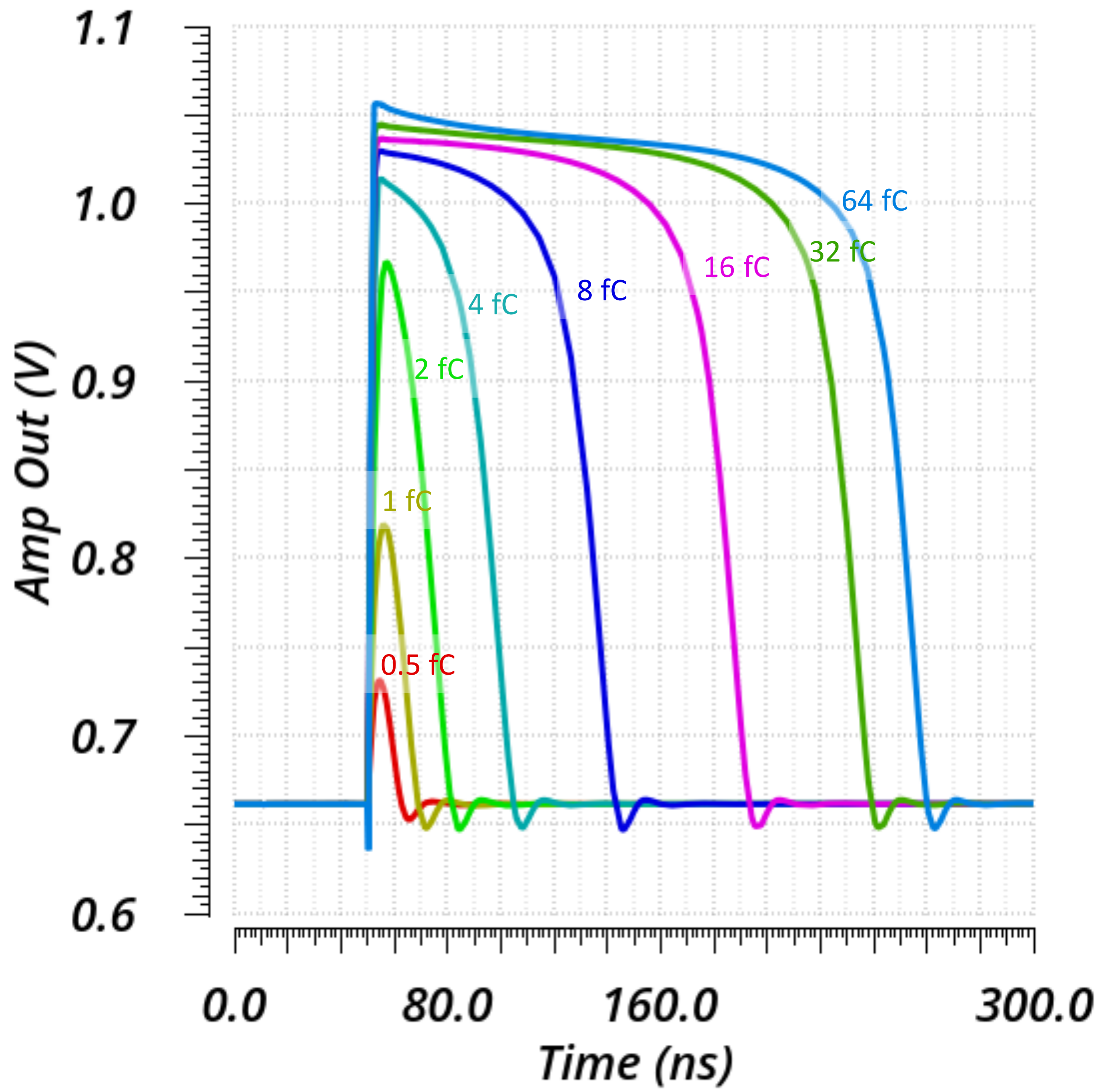


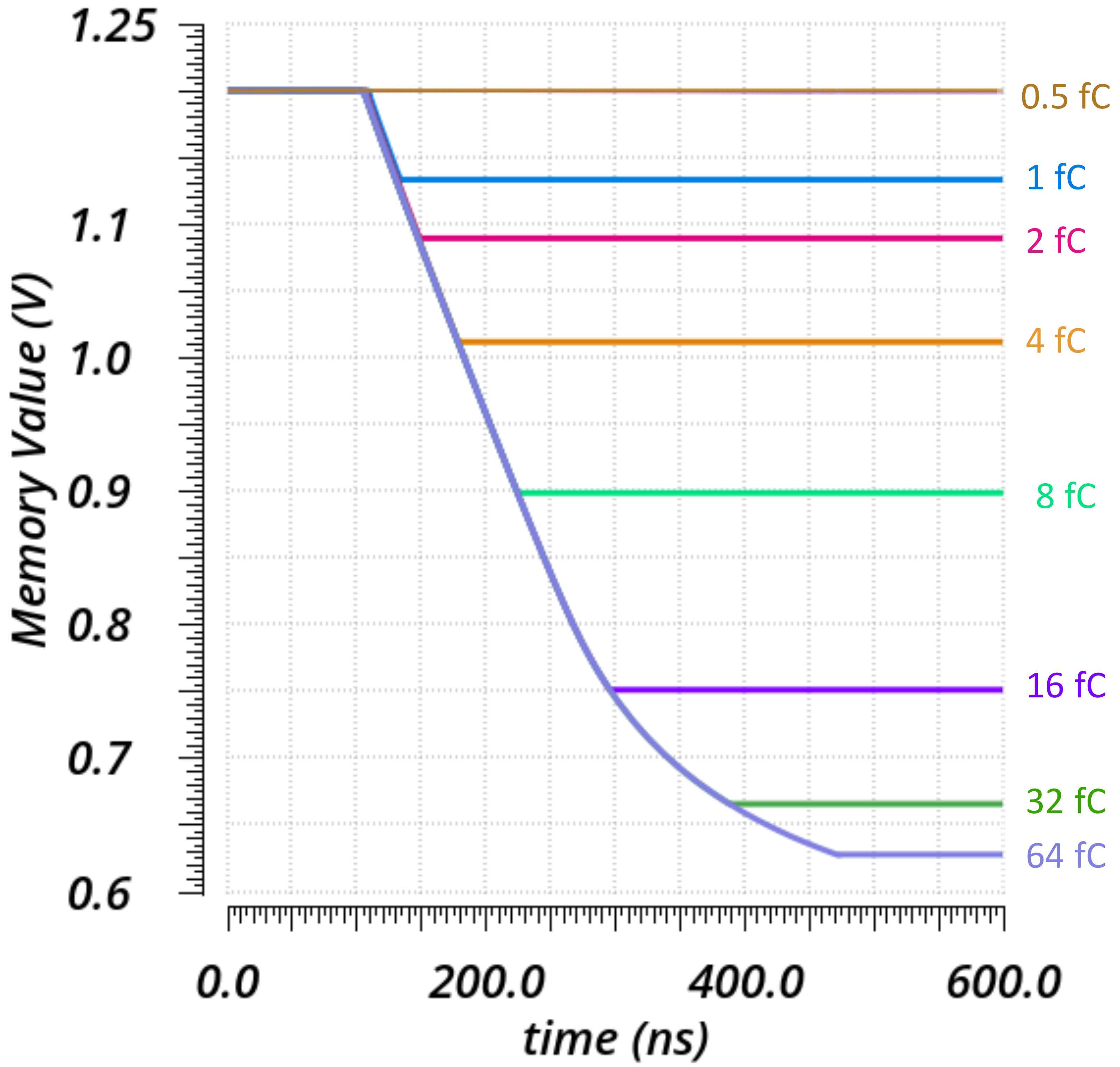
Monolithic Pixel ASIC: Charge Measurement

Analog memories: capacitors inside each pixel charged with const current during ToT

- =▶ when signal returns below threshold, memory is disconnected and left floating until read by flash ADC
- =▶ preamplifier designed to produce a signal proportional to the *log* of input charge

Simulation data





Pre-production Chip (2022)

Engineering run (IHP Microelectronics)

=▶ In each reticle, three pixel matrices

FASER_v1 (baseline)

↳ 128 x 64 pixels, 4 super-columns

↳ in-pixel pre-amp and driver

↳ discriminator outside

FASER_v2

↳ 128 x 48 pixels, 3 super-columns

↳ in-pixel pre-amp, driver, and discriminator

FASER_ALT

↳ 128 x 48 pixels, 3 super-columns

↳ no analog memories

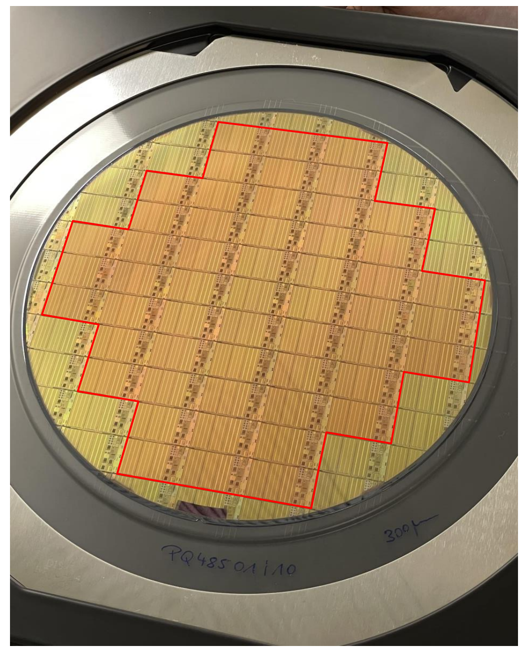
↳ counter for charge measurement

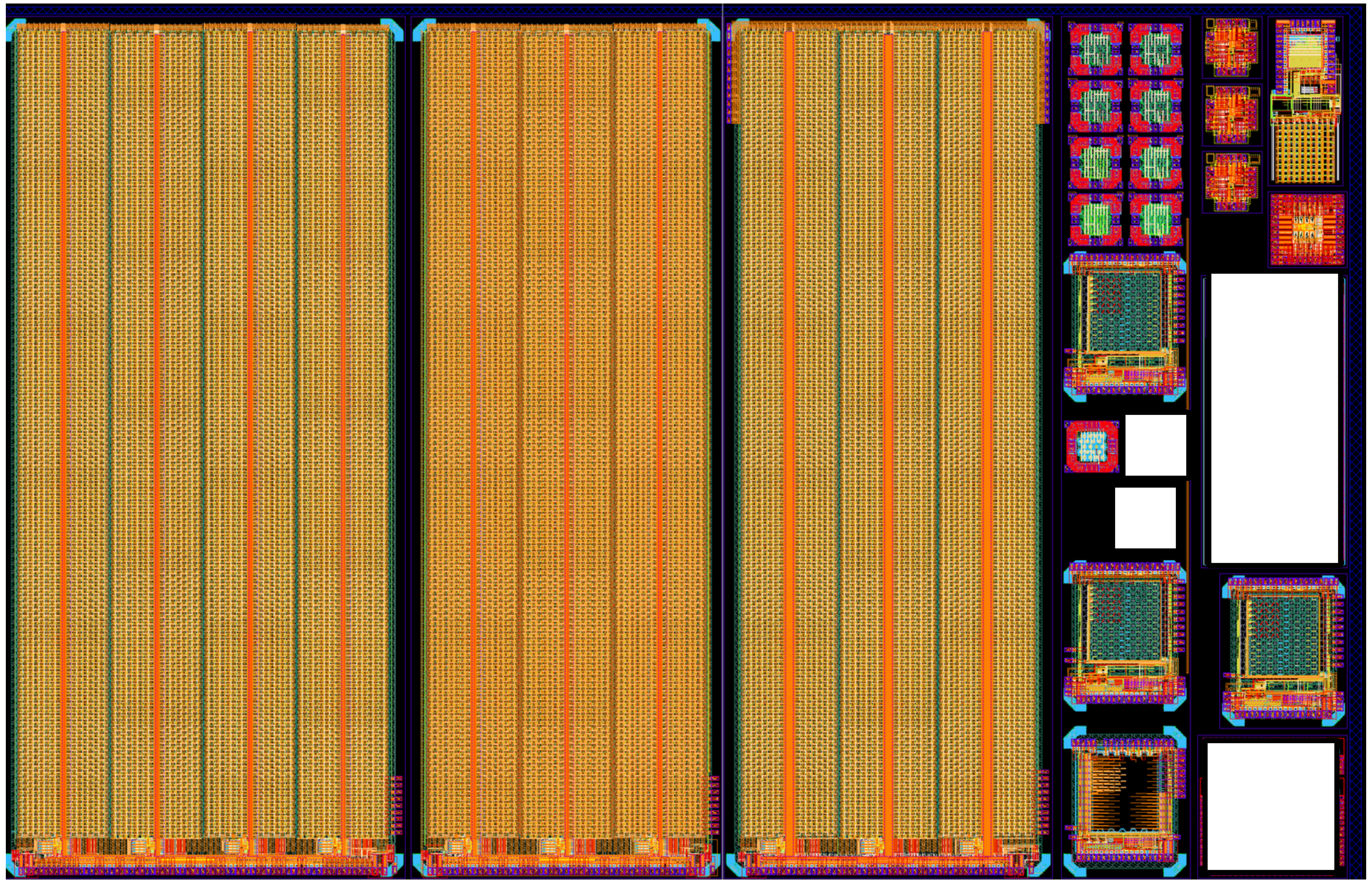
=▶ Several test structures (TDC, etc…)

Reticle: 2.4 x 1.5 cm^2

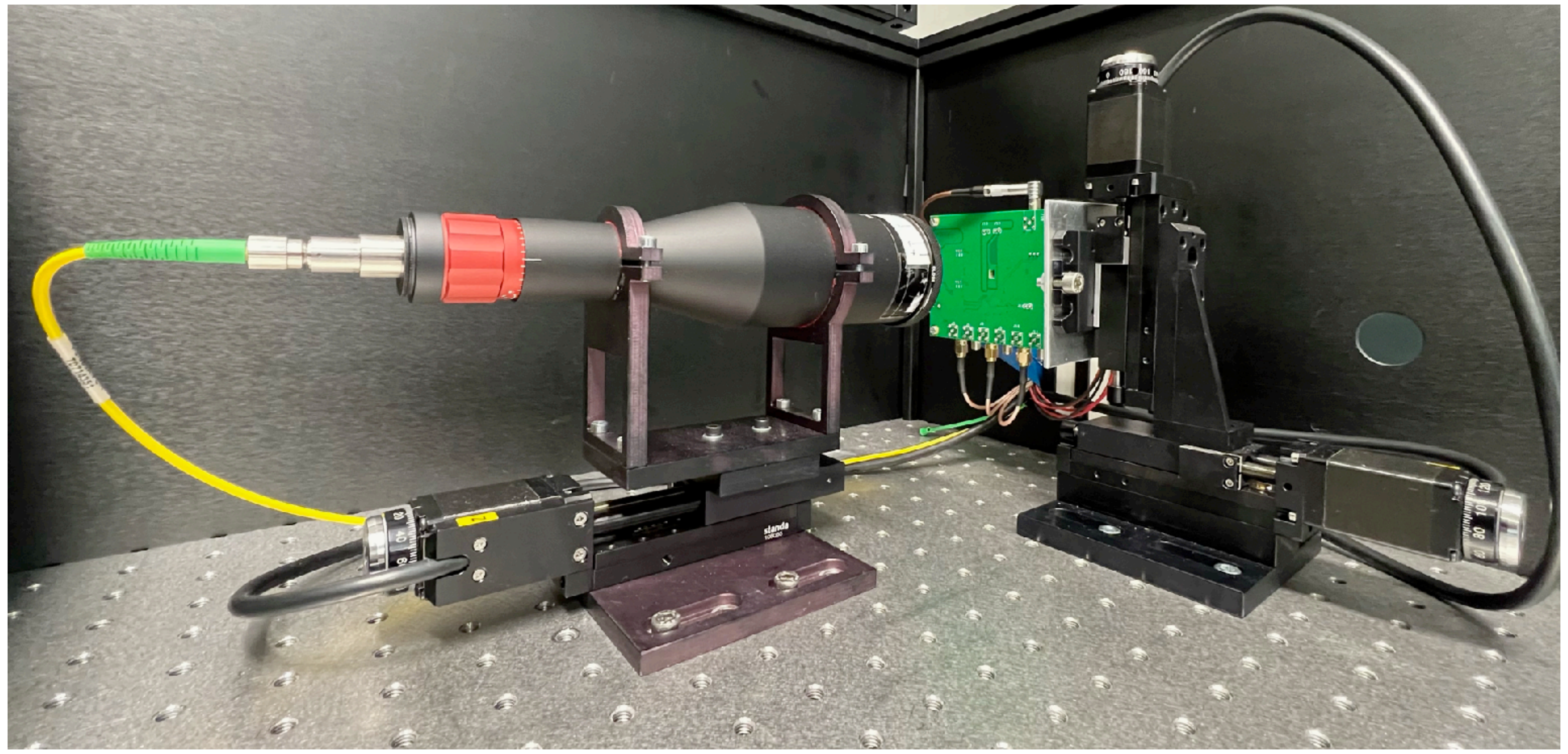
53 reticles per wafer

Thickness 300 μm



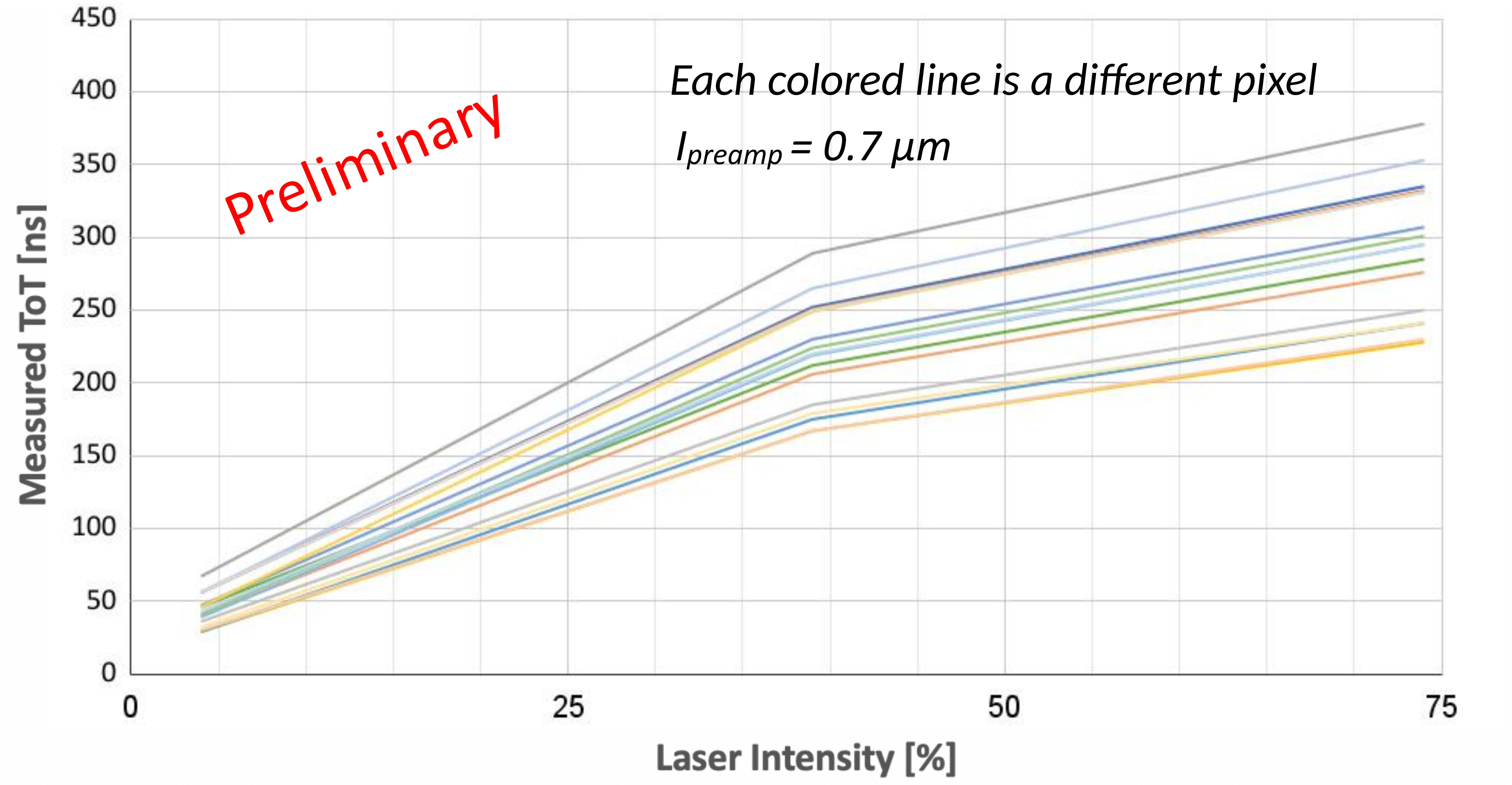


Pre-production Chip: TOT (Charge) Mismatch [I]



Evaluating charge response with infrared laser

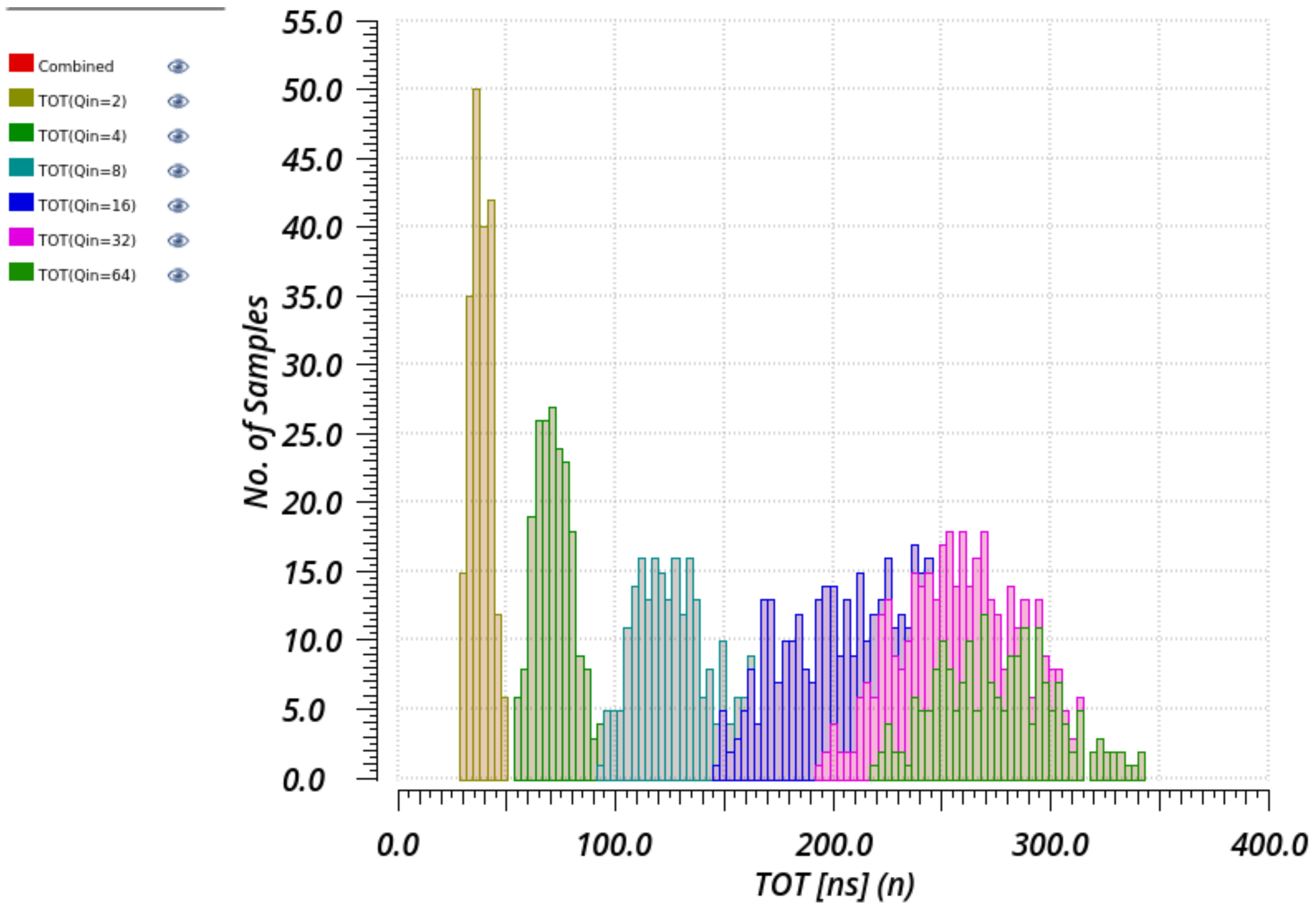
- measuring ToT via fast-OR signal on the scope
- varying per-pixel injected charge via laser attenuator
- measurement repeated at different I_{preamp}



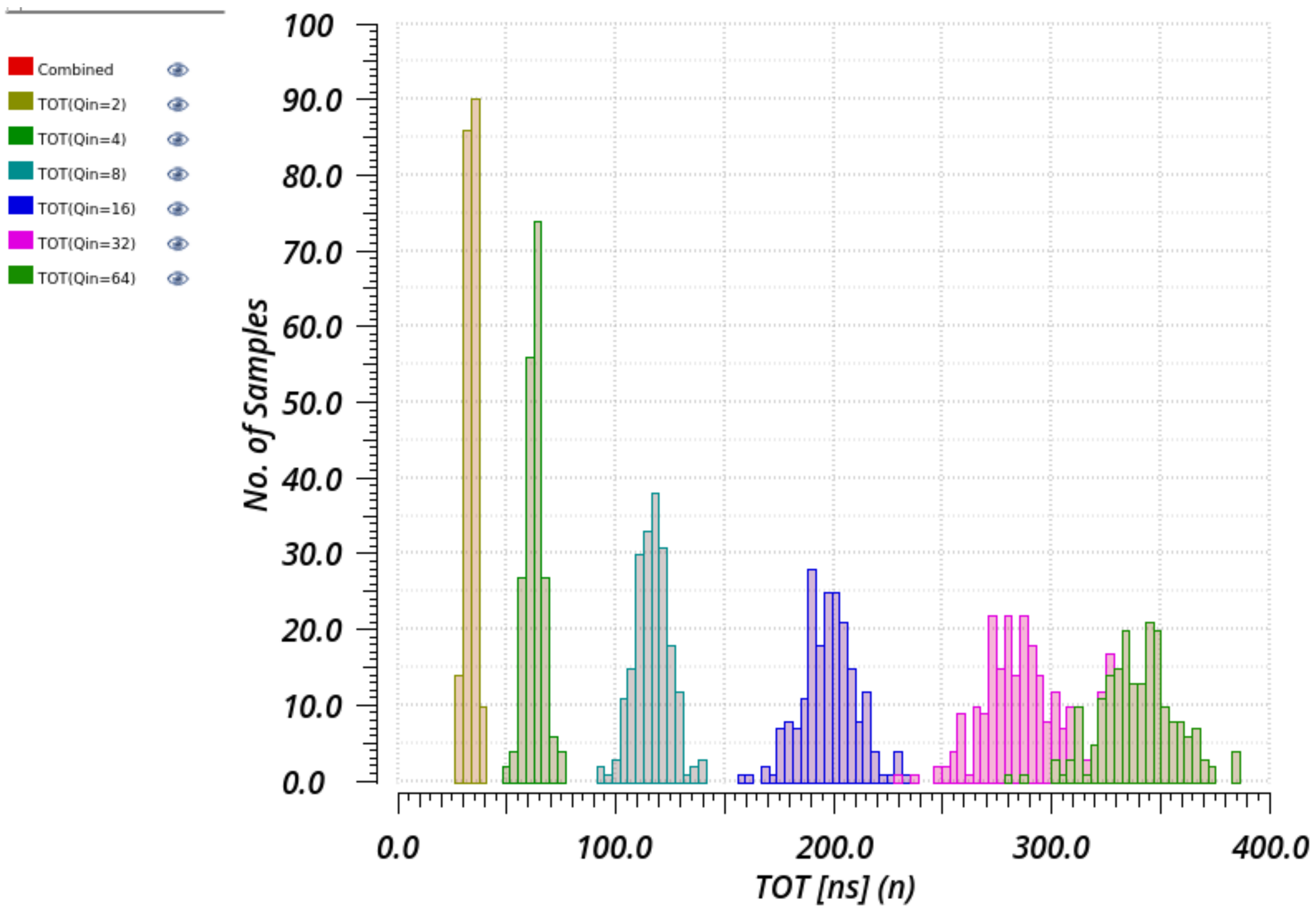
Pre-production Chip: TOT (Charge) Mismatch [II]

Expect improvement of front-end uniformity in production ASIC thanks to bigger transistors

Cadence Spectre Simulation:
front-end mismatch in <u>pre-reduction prototype</u>



Cadence Spectre Simulation:
front-end mismatch in <u>production ASIC</u>

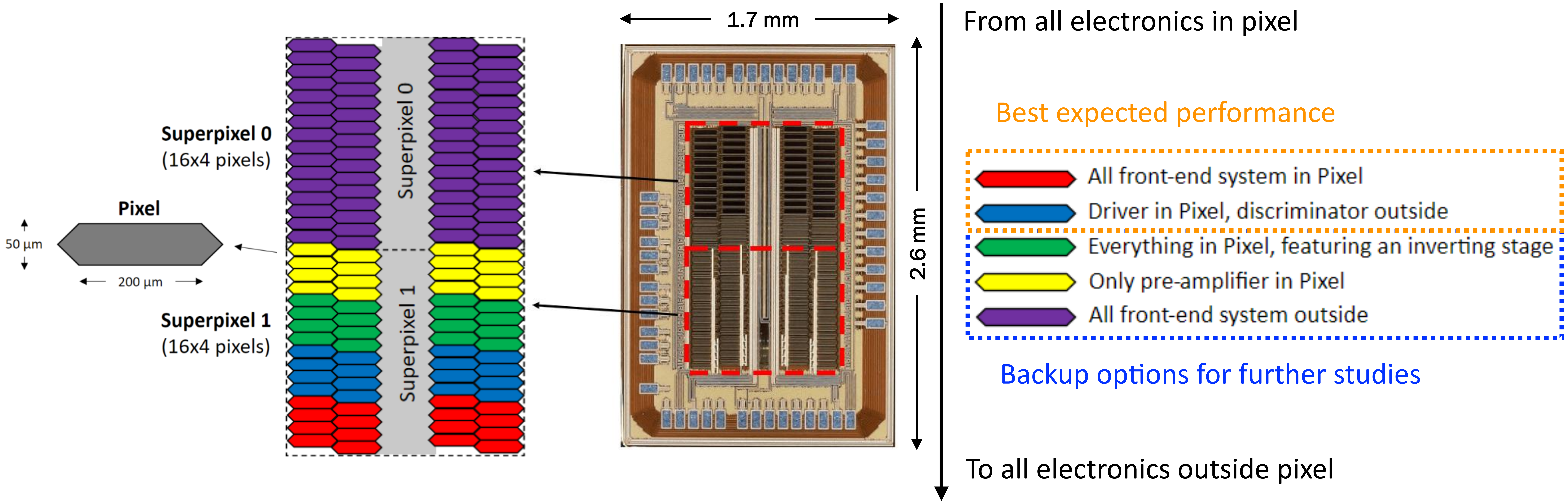


Small Prototype Chip (2021)

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

First chip prototype tested in 2021

- designed to study different levels of integration of front-end electronics
- simultaneous goals: minimize dead area and routing capacitance, maximize stability



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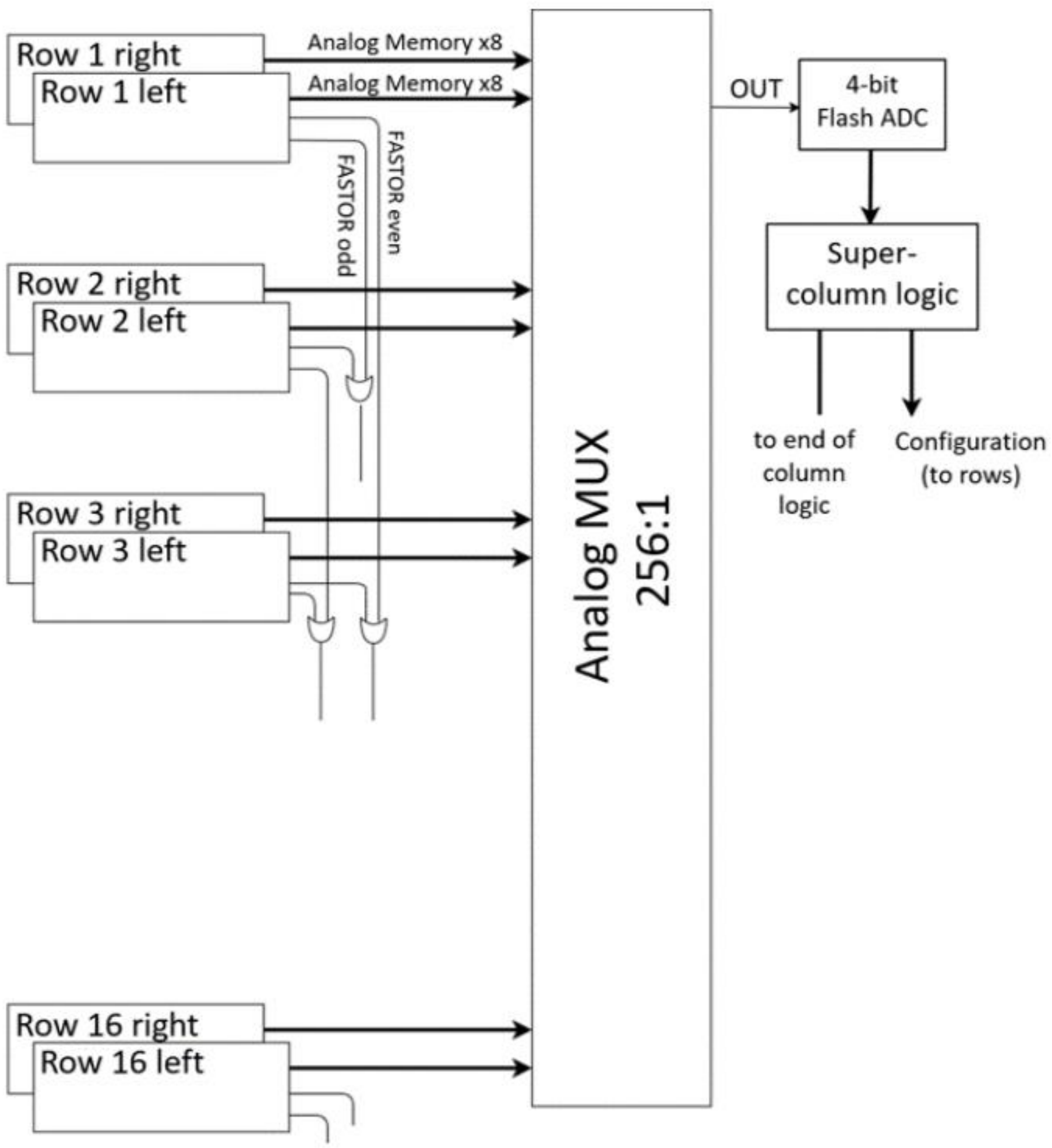
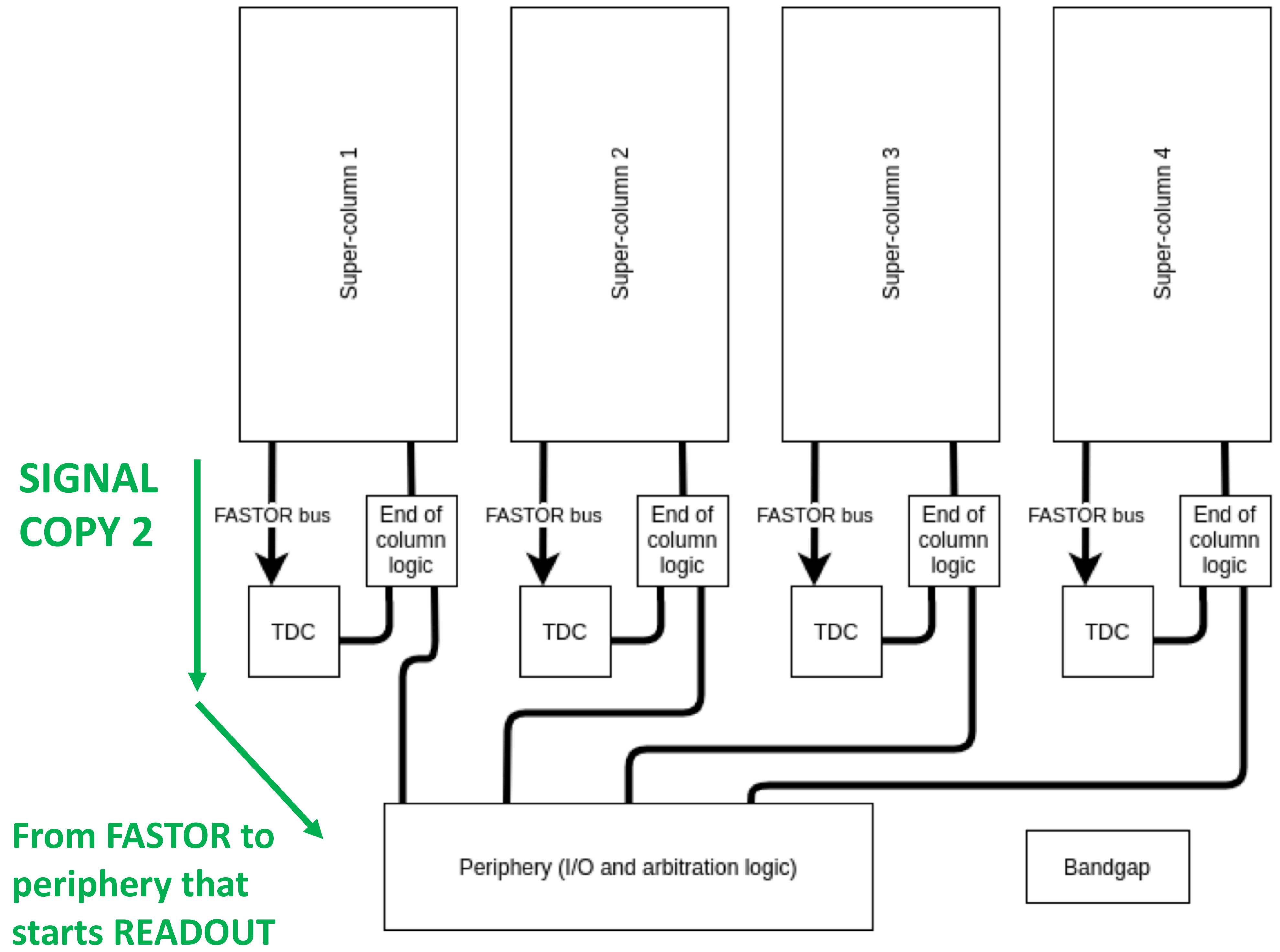
- designed to study different levels of integration of front-end electronics
- simultaneous goals: minimize dead area and routing capacitance, maximize stability

Configuration	σ_v [mV]	G_c [mV/fC]	ENC [e$^-$]	$\sigma_{V_{th}}$ [mV]
All f.e. outside pixel	4.2 ± 0.2	159 ± 1.0	165 ± 9	32.3
Only pre-amp. in pixel	2.5 ± 0.1	96.8 ± 0.5	161 ± 9	26.9
All f.e. in pixel, inv. stage	6.9 ± 0.5	179 ± 1.0	241 ± 19	30.8
Pre-amp. and driver in pixel	3.8 ± 0.2	133.7 ± 0.6	178 ± 9	23.4
All f.e. in pixel	5.4 ± 0.4	148 ± 1.0	228 ± 20	27.1

Last two configurations are good compromise between *compactness* and *performance*:
adopted for pre-production prototype

Monolithic Pixel ASIC: Charge Digitization & Readout





Periphery of matrix with three super-columns (from pre-production ASIC)